Performance analysis of Single Gate and Double Gate MOSFET with and without effect of noise

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Performance analysis of Single Gate and Double Gate MOSFET with and without effect of noise

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Dedicated
to
The Dreams and Sacrifices
of my Dear Ones
who Love me a Lot.

Declaration of Authorship

I, Sashmita Panda, declare that this thesis titled,"Performance analysis of Single Gate and Double Gate MOSFET with and without effect of noise" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
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Certificate

This is to certify that the thesis entitled **"Performance analysis of Single gate and Double gate MOSFET with and without effect of noise "** *by* **Sashmita Panda**, *submitted to the National Institute of Technology, Rourkela for the award of Master of Technology in Electrical Engineering, is a record of bonafide research work carried out by her in the Department of Electrical Engineering, under my supervision. I believe that this thesis fulfills part of the requirements for the award of degree of Master of Technology.The results embodied in the thesis have not been submitted for the award of any other degree elsewhere.*

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Abstract

In modern era, computing systems are designed to perform innumerable number of functions with high speed, low power consumption, less propagation delay, the number of circuits in a chip keeps increasing day by day. So, the electronics industry always faces the challenge of miniaturization of transistors which increases the package density and hence linear scaling of CMOS technology has become a necessity in the present day microelectronic and nano-electronic regime. This causes a problem for static power consumption and hence conventional MOSFETs fail to face the situation. Also Short Channel Effects (SCEs) come into picture while scaling the MOSFET. Hence non-conventional devices started gaining its significance to meet the ITRS requirements.

This thesis explains the performance analysis of Single Gate and Double Gate MOSFET with presence of noise. The performance of the MOSFET degrades when different noises come in to picture as compared to the previous MOSFET Model without noise. Also the behaviour of radio frequency (RF) DG MOSFET is analysed and verified up to 1MHz with measurements over a wide range of bias voltages and channel lengths. Significant variation in the noise spectral density has been observed.

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List of Symbols

Acronym	Description
Vth or VT	Threshold Voltage
VGS or Vgs	Gate to Source Voltage
VDS or Vds	Drain to Source Voltage
Ids or ID	Drain Current
Tox or tox	Gate Oxide Thickness
Lg or L	Channel Length
ni	intrinsic carrier concentration of Si
K	Boltzmann's Constant
T	Temperature in Kelvin
EC	Electron Affinity
EG	Energy Band Gap
	Body Factor
SiO2	Silicon Dioxide
SiGe	Silicon Germanium
Si3N4	Silicon Nitride
HfO2	Hafnium Oxide
VSat	Saturation Velocity
VFB	Flat Band Voltage

List of acronyms

List of acronyms

Acronym	Description
ITRS	International Technology Roadmap for Semiconductors
CMOS	Complementary Metal-Oxide Semiconductor
FET	Field Effect Transistor
SOI	Silicon on Insulator
FD-S-SOI	Fully Depleted Strained Silicon on Insulator
DG MOSFET	Double Gate Metal-Oxide Semiconductor Field Effect Transistor
SS	Sub-threshold Slope
DIBL	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
SCEs	Short Channel Effects
GS	Gate Stack
FD-S-GS-DG	Fully Depleted Strained Gate Stack Double Gate
2-D	Two Dimensional
SiGe	Silicon Germanium
TFP	Silicon Germanium
GTFP	Gain Transconductance Frequency Product
GFP	Gain Frequency Product
FOM	Figure of Merits
TGF	Transconductance Generation Factor

Chapter 1

Introduction

1.1 Motivation

The demand for low-power and high-speed circuits, and development of device fabrication technology continue to drive the scaling down MOS devices under $0.1\mu m$ channel length. Now a days, many CMOS circuits are operated with 1.2V supply voltage and some are running in GHz range of operating frequency. At this level of device scaling, some dimensions of the MOS device, such as gate thickness became comparable to atomic dimensions, hence quantum mechanical corrections in device simulation are indispensable.[1]. Also, the operating voltage cannot be scaled down with the same ratio as that for the device in order to maintain adequate threshold voltage that limits leakage current within a reasonable level, therefore the electric field in the device become so large that accelerated carriers can have kinetic energy more than ten times than that thermal energy.[2].
The supply voltage also scales down with device scaling, however, it cannot follow the speed of channel length reduction. Therefore, the maximum electric field for a minimum size MOS transistor rises to the tens of volts/μm level. The carriers in the device are accelerated by this electric field and acquire excessive kinetic energy. These high energy carriers are called hot carriers because they have effective temperatures of several thousands of carrier temperatures[3]. To extract parameters of such scaled devices for circuit simulations, AC simulations accounting for advanced transport effects are required[4]. Thismodel is also useful for noise simulations, where the carrier energy has an important role in noise generation[5].The noise parameters in a short channel MOS device are reported to increase as the channel length scales down. However, the amount and origin of the increased noise is still debatable.

1.2 Semiconductor Technology Scaling : A Historical Overview

The central component of semiconductor electronics is the integrated circuit (IC), which combines the basic elements of electronic circuits such as transistors, diodes, capacitors, resistors and inductors on one semiconductor substrate. The two most important elements of silicon electronics are transistors and memory devices. For logic applications MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are also used. The basic structure of Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is shown in Figure 1.1. The continuous research in semiconductor devices and its application in technological growth reinforced each other and soon scaling of the semiconductor devices became most challenging task[6].

1.2.1 Reasons for MOSFET Scaling

Smaller MOSFETs are preferable for several reasons. The major reason for making transistors smaller is to pack more and more devices in a given chip area which results in a chip of similar functionality in a small area, or chips with more functionality in the same area. Smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 40 years the number of transistors per chip has been doubled every 23 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as many as in a 65 nm chip[7].

1.2.2 MOSFET Scaling

In the forty-five years since 1965, the price of one bit of semiconductor memory has dropped 100 million times. The cost of a logic gate has also undergone a same dramatic drop. The primary engine that powered the proliferation of electronics is miniaturization. By making the transistors and the interconnects smaller, more number of circuits can be fabricated on each silicon wafer and hence each circuit becomes cheaper.

Constant Field Scaling Theory

- Vertical dimension decreases with same lateral dimensions.
- To maintain fixed electric field, operating voltage decreases.

Constant Voltage Scaling Theory

- Attractive due to electrical compatibility with existing circuit.
- Vertical dimension decrease quadratically relative to the lateral dimensions.

Table 1.1: MOS Scaling Theory

Parameter symbol	Gate Length	Constant Field Scaling	Constant Voltage Scaling
Gate Length	L	$1/\alpha$	$1/\alpha$
Gate Width	W	$1/\alpha$	$1/\alpha$
Electric Field	E	1	A
Oxide Thickness	T_{OX}	$1/\alpha$	$1/\alpha$
Substrate Doping	N_a	$/\alpha 2$	$/\alpha 2$
Gate Capacitance	C_g	$/\alpha 2$	$/\alpha 2$
Oxide Capacitance	C_{OX}	$/\alpha$	A
Voltage	V	$1/\alpha$	1
Current	I	$1/\alpha$	A
Power	P	$1/\alpha 2$	A

So a trade-off among performance, yield, and compatibility with existing technology, reliability, process complexity, device performance and impact of parasitic must be made when selecting a scaling strategy.

1.2.3 Moores law

Moores Law states that the number of transistors on integrated circuits doubles every two years, as shown in Figure 1. It is observed that that Moores Law cannot be sustained forever. However, predictions of size reduction limits due to material or design constraints, or even the pace of size reduction, have proven to elude the most insightful scientists.

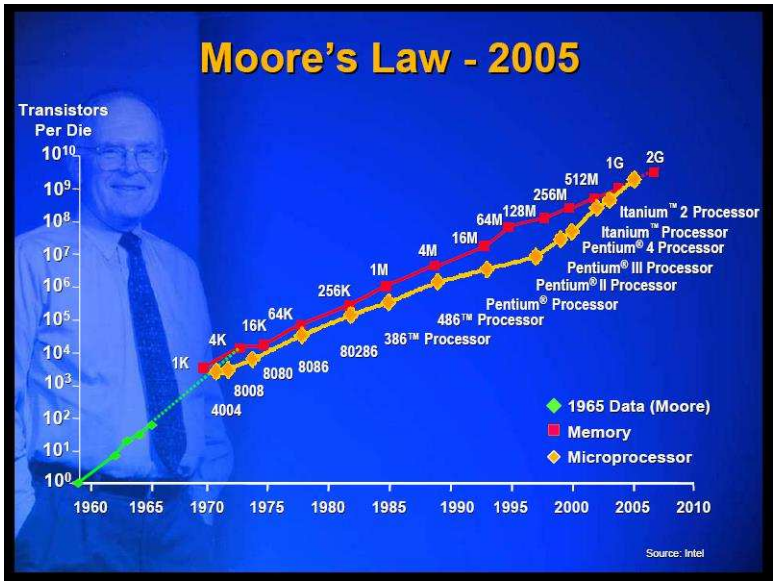

Figure 1.1: Moores law

1.3 Types of Scaling

1.3.1 Full Scaling(Constant Field Scaling)

In this type of scaling, both the horizontal and vertical dimensions are scaled down by $1/S$ where S is scaling factor. As the electric field which is the ratio between voltage and distance need to be constant, all the voltages also need to be scaled down by $1/S$ .In this kind of scaling the threshold voltage is also scaled down by $1/S$. Hence this scaling results in reduction of current which in turn reduce power. But power density remains constant as there is an increase in the number of transistors per unit area[8].

1.3.2 Constant Voltage Scaling

In this method both horizontal and vertical device dimensions are scaled by S, but all the operating voltages are constant and thus there would be an increase in the electric fields in the device.In this case the threshold voltages would be constant and the power per transistor increases by S. Here increased level of doping required for preventing channel punch through makes this type of scaling mostly impractical[9].

1.3.3 General Scaling

In general scaling, device dimensions will be scaled by a factor of S and the voltages will be scaled by another factor of U. The speed of the circuit can be improved by general scaling technique these type of devices would be energy efficient as well as reliable.So the technology advancements witnessed by todays world have resulted in efficient monolithicICs with novel transistors as switching elements and this had resulted in ICs that are considerably faster and highly complex to handle multiple functions[**?**].

1.4 Power consumption in the electronic industry

Over the past four decades, there has been an increasing trend in the power consumption of lead microprocessors. In 1974, NMOS was preferred to PMOS due to its advantages like speed and area. But due to lower noise margins and static power consumption (DC) of NMOStechnology, it was no longer used in the industry from 1980s. CMOS technology exhibits low intrinsic power dissipation and superior scaling characteristics and hence dominated IC industry in 1980s. But the rate at which chip area grows is much smaller as compared to the rate at which the number of transistors as well as power density grows.

$$Staticpowerconsumption = I_{LEAK} * SupplyVoltage$$

where I_{LEAK} is the sum of the leakage currents of MOSFET in OFF state.

$$Dynamicpowerconsumption = f * C_L * SupplyVoltage$$

where f is the frequency, C_L is the load capacitance. It is seen that if supply voltage is not scaled down, there will be an increase in power density. Increase in power thus results in reduced battery life, more heat production and proves to be economically and environmentally less friendly. So there is a significant challenge posed due to power consumption in designing IC systems.

1.5 Limitation due to Scaling of conventional MOSFETs

Various setbacks posed by scaling conventional MOSFETs are;

1.5.1 Channel Length Modulation

When the MOSFET is scaled down to lower dimensions, inverted channel shortens as drain bias is increased thus giving rise to channel length modulation which in effect increases drain current for a MOSFET which operates in saturation as well as reduces output resistance of MOSFETs. The shortening of channel region happens due to extension of the non-inverted region towards source as drain voltage is made high. Hence reduction of output resistance happens due to decrease in length thus causing an increased drain current[**?**].

1.5.2 Short Channel Effects (SCEs)

A semiconductor device is known to be a short channel device when its channel length becomes comparable to drain depth and source depth as well as depletion width. MajorSCEs are;

Velocity Saturation of Carriers

When the MOSFETs are scaled down to very low dimensions, the charge carriers experience very strong electric fields because of which their velocity reaches a maximum and saturates thereby, there would be no longer increase in carrier velocity when applied electric field is increased further. This phenomenon provides limitation for carrier movement in semiconductor and is hence called velocity saturation effect which is one of the major SCE.

Drain Induced Barrier Lowering (DIBL) and Punch Through

In small channel MOSFETs, at comparatively high drain voltages, threshold voltages reduces unlike long channel devices where threshold voltage is independent of drain voltage. This phenomenon happens in short channel MOSFETs as drain voltage is increased, the depletion region of the drain-body junction extends under gate and barrier lowering of electrons in channel takes place and threshold voltages reduces. Hence this effect is named as as Drain Induced BarrierLowering (DIBL). When the drain as well as source depletion regions combine together, the gate voltage will not be able to control the current flow and this condition is coined as punch through.

Surface Scattering

In small channel dimensions, vertical component of electric field accelerate electrons towards the surface which undergo collision and faces difficulty as they move through the channel. This limits the mobility of electrons and the phenomenon thus named surface scattering.

Impact Ionization

Due to the presence of very longitudinal electric field in short channel MOSFETs, electrons have higher velocity, which impacts silicon atoms and ionize them and can create electron hole pair. This phenomenon worsens when electrons due to high fields, travel to substrate while trying to escape from the drain region and hence can affect the adjacent devices on the chip.

Hot-Carrier Injection

A mechanism that can change the switching characteristics permanently for a transistor, where an electron as well as a hole can gain high kinetic energy and enter into the dielectric of the MOSFET.. This makes semiconductor devices less reliable.

1.5.3 Narrow Channel Effect

In small channel width devices, depletion region in the channel region is larger compared to what is assumed. This takes place due to fringing fields. Hence due to narrow channel, threshold voltage of the device increases.

1.5.4 Subthreshold Conduction

Subthreshold conduction is the drain current between source and drain in thesubthreshold region of MOSFET. As MOSFETs are scaled down to nanometreranges, voltages also gets scaled down and sub threshold leakage increases and may led to 50Hence conventional MOSFETs cannot be looked upon as the device of future semiconductor world as it can be optimized to a certain limit only. The Subthresholdswing of conventional MOSFETs has a minimum limit of 60mV/decade. MOSFETs have I_{ON} to I_{OFF} ratio in the order of 103 to 104 .So device engineers go forward with non conventional devices withSubthreshold swing less than 60mV/decade and higher I_{ON} with very negligible I_{OFF} trying to make them behave as ideal switch.

1.6 Introduction to noise sources

1.6.1 Definition of Noise

Noise is a spontaneous fluctuation in current or in voltage which is generated in all semiconductor devices. The intensity of these voltage fluctuations or current fluctuations depends on device type, its manufacturing process, and operating conditions. The resulted noise is the combination of different noise sources, which is called as an inherent noise. The inherent noise can also be used as the quality assessment of semiconductor devices. Often it has been used as an important factor during the development of the production process of new semiconductor devices. The important sources of noise are thermal noise, shot noise, generation-recombination noise, 1/f noise (flicker noise), 1/f2 noise, burst noise or random telegraph signal (RTS) noise and avalanche noise etc. In general, the analysis of the noise performance of the transistors is critical for developing low-noise applications with a reduced cost. Due to the randomness of noise, we need to use statistical approaches for its characterization. Generally, the average of noise current is zero, hence the power spectral density of noise per unit frequency is used for the expression of noise[10].

1.6.2 Intrinsic noise sources in Semiconductor Device

The intrinsic noise in a semiconductor device is generated by several different mechanisms. Due to the difference of these mechanisms, the frequency behaviour of noise becomes complex. Several major noise generation mechanisms in MOS transistors are reviewed here.

Thermal Noise

Thermal noise is also known as Johnson-Nyquist noise from the name of researchers who first measured and empirically determined to the equation of thermal noise [1]. It is also called diffusion noise in non-equilibrium conditions. The scattering of electrons with the surrounding lattice makes them have random motion, and this randomness appears as thermal noise at electrodes. Thermal noise is caused due to the heating effect effect of the device.Generally heating effect occurs due to the accumulation pf charge carriers.

Generation-Recombination Noise

Generation-recombination (GR) noise is caused due to fluctuation in the number of carriers inside of a two terminal sample associated with random transition of charge carriers between states in different energy bands. It represents a typical noise source in semiconductor where carrier concentration can vary over many orders of magnitude. Some examples of transitions are between conduction band and localized levels in the energy

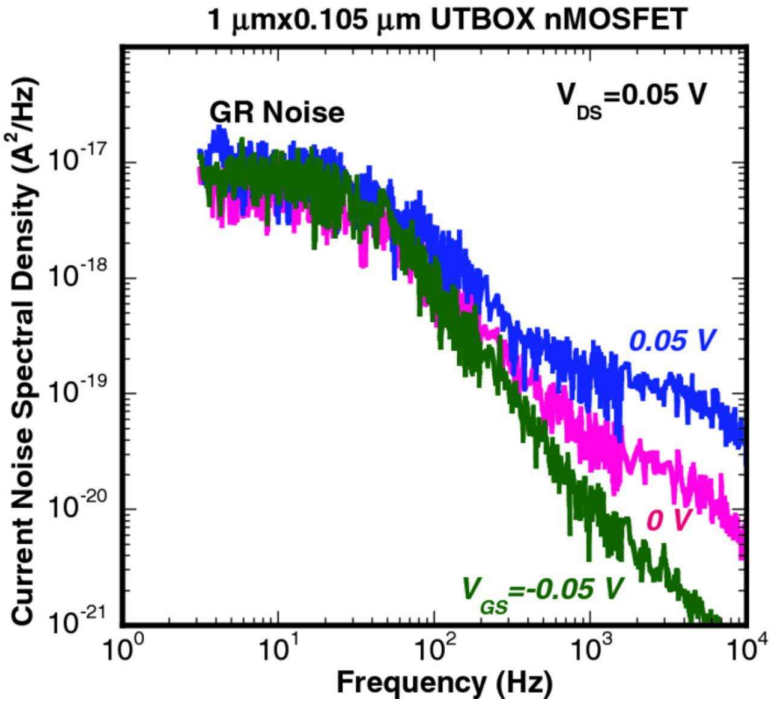

Figure 1.2: Low frequency noise sources in MOS structure

gap, conduction and valence band etc. Therefore, GR noise is inherently due to fluctuation of carrier number, usually keeping charge neutrality of the total sample.

Flicker $(1/f)$ noise

Although many researchers studied flicker noise for a long time, the exact mechanism is still uncertain. Flicker noise of a MOS transistor is assumed to originate from inter-facial oxide traps[10]. At the interface between oxide and silicon, many dangling bonds appear creating available energy states. These inter-facial oxide traps randomly trap and release charge in the channel. Flicker noise cannot be modelled easily because it is generated from surface defects which depend on the CMOS fabrication process. Also, PMOS transistors are generally observed to generate less flicker noise than NMOS transistors because the buried channel in PMOS transistors helps the holes to maintain some distance from inter-facial traps. A typical 1/f noise model of a MOS transistor has following form[11].

1.7 Objectives

The main objective of this thesis is to investigate performance of the MOSFET in presence of noise and also study the behaviour of radio frequency (RF) DG MOSFET is analysed and verified up to 1MHz with measurements over a wide range of bias voltages and channel lengths. Significant variation in the noise spectral density has been observed.

1.8 Thesis Outline

The remaining part of the work is broadly divided into seven chapters each with multiple sub sections. Each chapter can be summarized as follows. CHAPTER-2 is a Literature review in which the performance analysis of single gate and double gate MOSFET has been done. Also this chapter explains about the effect of noise in single gate and double gate MOSFETs. CHAPTER-3 this part begins with the TCAD Software and its various features. It also briefs about the different tools of the TCAD Software used in the current simulation work. CHAPTER-4 summarizes the analysis of DC and analog/RF performance of DG MOSFET by varying

the gate length, work function, and high-K dielectric. CHAPTER-5 explains the performance comparison between UTB-SG and DG-MOSFETs with Si and III-V channel materials by varying channel length and doping concentration. CHAPTER-6 summarizes about the Thermal noise analysis of single gate MOSFET at high frequency by varying channel length and silicon thickness. CHAPER-7 explains about the Thermal noise analysis of double gate MOSFET at high frequency by varying channel length and silicon thickness. CHAPTER-8 concludes the thesis and mentions the scope for future work.

1.9 Summary

Continuous scaling in MOSFET devices degrade the performance of the device resulting in major problems such as leakage currents and short channel effects (SCEs) are major problems. To overcome these problems, a device called SOI MOSFET has been developed. To increase the density and enhance the performance of CMOS technology new materials are introduced into the classical single gate MOSFET and non-classical multi gate MOSFETs are developed. For higher current drive, faster and smaller chips, the bulk MOSFET scaling is a traditional process. By reducing the channel lengths in each next technology node, the improvement in performance and reduction of cost is achieved. But in recent years, the MOSFET scaling is slowed down; hence people are searching for new technologies /methodologies.

Chapter 2

Literature Review

SOI Transistor An SOI MOSFET is a semiconductor device (MOSFET) where a semiconductor layer such as silicon or germanium is developed on an insulator layer which may be a buried oxide (BOX) layer formed in a semiconductor substrate. SOI MOSFET devices are adapted for use by the computer industry. There are two types of SOI devices such as a) PD SOI (Partially depleted silicon on insulator) and b) FD SOI (Fully depleted silicon on insulator). For an n-type PDSOI MOSFET the sandwiched p-type film between the

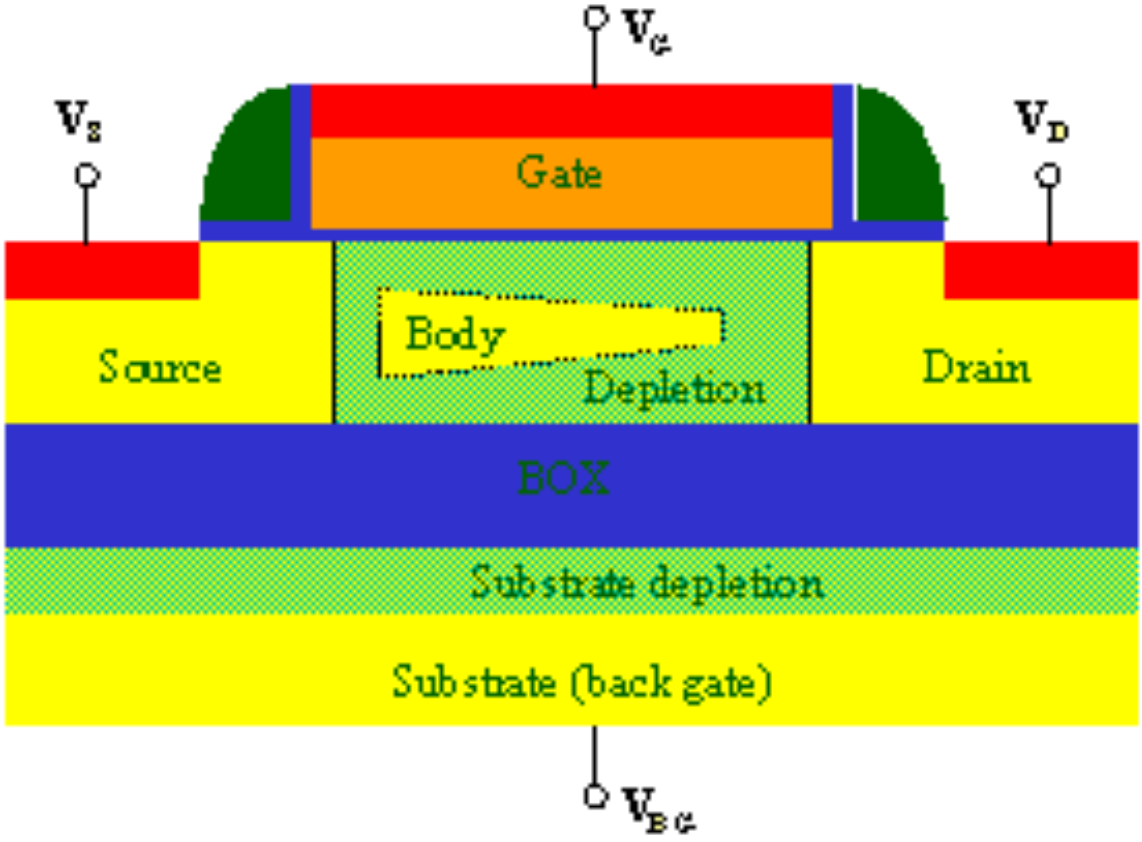

Figure 2.1: Partially Depleted SOI

gate oxide (GOX) and buried oxide (BOX) is large, so the depletion region can't cover the whole p region. So to some extent PDSOI behaves like bulk MOSFET. Obviously there are some advantages over the bulk MOSFETs. The film is very thin in FDSOI devices so that the depletion region covers the whole film. In case of FDSOI the front gate (GOX) supports less depletion charges than the bulk so an increase in inversion charges occurs resulting in higher switching speeds.
In 1999, S. C. Williams has published a paper in which he has explained that the fully depleted

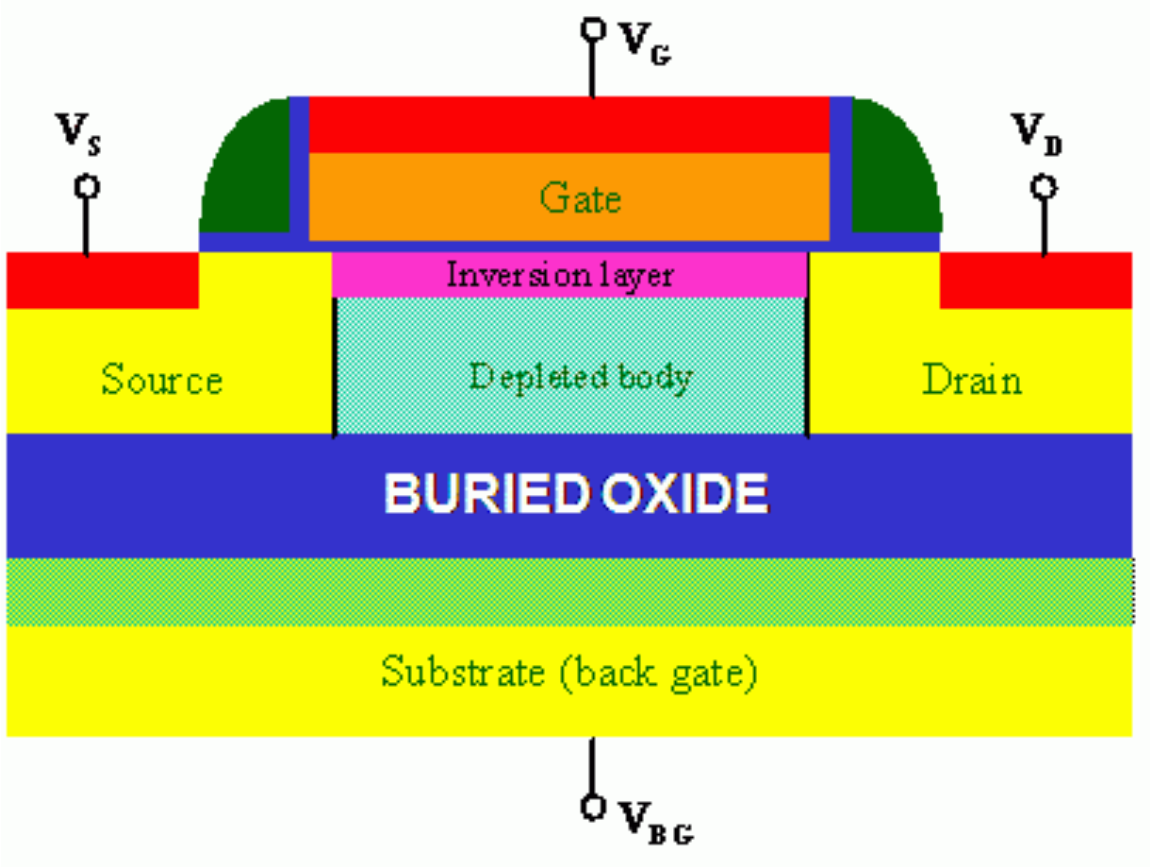

Figure 2.2: Fully Depleted SOI

silicon-on-insulator (FD SOI) MOSFET offers impressive advantages over bulk counterparts, including increased drain current, improved sub threshold slope, high trans conductance, and immunity to short-channel effects. Advanced FD SOI devices, such as the double-gate (DSOI) design, have demonstrated even greater performance than single-gate (SSOI) devices (e.g., nearly ideal sub threshold slope and greater drain current).

2.1 Single Gate and Double Gate MOSFET

Double Gate MOSFETs using lightly doped ultrathin layers seem to be a very promising option for ultimate scaling of CMOS technology. Excellent short-channel effect (SCE) immunity, high trans conductance, and ideal sub threshold factor have been reported by many theoretical and experimental studies on this device. This structure utilizes a very thin body to eliminate sub-surface leakage paths between the source and drain, and thereby provides excellentundoped body is desirable for immunity against dopant fluctuationeffects which give rise to threshold-voltage variation, and also for reduced drain-to-body capacitance and highercarrier mobility which provide for improved circuit performance. The threshold voltage of a lightly doped DGMOSFETis can be adjusted by tuning the work function of the gate material.
In 2000,Digh Hisamoto has introduced a self-aligned Double-Gate MOSFET scalable to 20nm, where Self aligned double gate effectively suppresses SCEs, even with 17nm gate length.Si0.4 Ge0.6 gate provides a proper threshold voltage for ultrathin body MOSFET. Gate is self-aligned to the S/D which is raised to reduce the parasitic resistance. In 2005, Ali A.Orouji,M.Jagadish Kumar has published a paper where he has told that DG structure effectively reduce the SCEs due to suppression of the charge sharing by the inversion layer under the side gates. He has suggested that Suggests that the Optimized side gate length condition in terms of SCEs and the hot carrier effect is achieved when the side gate length is equal to the main gate length.In 2008,Pedram Razavi1, Ali A. Orouji2 suggested that Double-gate MOSFETs are suitable structures for suppressing short channel effects and are one promising candidate for nanoscale regime. Since decreasing

the dimension of the device needs simultaneous decreasing of the oxide thickness, gate tunnelling current is an issue in sub-100nm regime. Gate leakage current increases exponentially with decreasing gate oxide (SiO2) thickness. To overcome the limitation of the gate oxide thickness, using high-k materials in oxide could be useful. Since, higher gate dielectric thickness leads to higher fringing field, using of gate oxide stack will be desirable.In 2011, Ramesh Vaddi, S.Dasgupta, R.P.Agarwal has proposed that DGMOSFETs can either have a three terminal (3T) configuration, where both the gates are tied, or a four-terminal (4T) configuration, where the back-gate bias is fixed and the front gate acts as the control electrode independent of back gate bias. There are four types of DGMOSFETstied gate symmetric DG, tied gate asymmetric DG, separated gate symmetric DG, and separated gate asymmetric DG. The asymmetrical DGMOSFET can be achieved by applying different gate voltages, by different oxide thickness for front and back gates, by different gate material work functions or by all the options.

2.2 Effect of noise in SG and DG MOSFET

A fully depleted double gate (DG) silicon-on-insulator (SOI) is regarded as a near ideal technology, offering a higher drive current than its single gate (SG) counter part due to larger control over channel region, and this strongly enhances the immunity towards the short channel effects (SCEs) and provides an almost ideal sub-threshold slope. In 2011,Indra Vijay Singh, M.S. Alam has explained that after addition of noise in single gate MOSFET and double gate MOSFET, double gate MOSFET gives better performance in noise figure. In this paper, the DC, RF and noise properties of DG and SG SOI MOSFETs have been described. A systematic analysis technique for the two structures is presented based on surface potential formalism and the channel segmentation technique for small-signal and noise analysis. The noise performance of double-gated and single-gated MOSFETs is compared. We found a noticeable improvement of the noise figure in the DG structure that is explained interns of a favourable increase of cross-correlation between the Drain and gate currents. Finally, we show that the presence of a residual undesired charged impurity in the channel of a DG Structure induces perceptible changes in the spectral density of the gate current fluctuations that modifies the noise figure[11].
In 2011,Massimiliano Pierobon,Ian F. Akyildiz, has proposed a diffusion based Noise analysis for molecular communication in nanonetworks. It focuses on the diffusion based architecture as it represents the most general and widespread molecular communication architecture found in nature. In 2014,A. Monisha, R.S Suriavel Rao has explained that Double gate devices are preferred for its suppression of short channel effect, low leakage current and better sub-threshold characteristics. The germanium on insulator based devices has high degree of short channel effect than the silicon on insulator based MOSFETs.

2.3 Problem Statement

Comparative Study of performance in Single and Double Gate Nano Scale SOI MOSFET with the effect of noise.

2.4 Past Work

Various researches have been done in investigating the performance of the MOSFET in presence of noise. It has been seen that the performance of the MOSFET decreases in presence of noise. In 2011,Indra Vijay Singh, M.S. Alam has explained that after addition of noise in MOSFET, performance decreases as compare to previous MOSFET Model. He has also investigated the comparative performance analysis between single gate and double gate MOSFET in presence of noise. It has been found that Double gate MOSFET gives better noise figure as compare to Single gate MOSFET.

Chapter 3

Performance comparison of Ultra-Thin Si Directly on Insulator (SDOI) MOSFETs at specific Gate length

3.1 Introduction

CMOS devices come to nanoscale regime to acquire higher density and low power consumption. The inauspicious effects cause threshold voltage variation with higher leakage current in nano devices known as short channel effects (SCEs). Due to these SCEs the conventional scaling comes to an end, but to maintain the Moores law research going towards inventions of novel devices. As the natural length of the device[12].

$$\lambda = \sqrt{\frac{\varepsilon_{si}\, t_{si}\, t_{ox}}{n\, \varepsilon_{ox}}}$$

permittivity of S_i, ϵ_{ox} permittivity of oxide, t_{Si} and t_{ox} thickness of Si body and oxide. λ is the measure of SCEs and it should be as small as possible to minimize the SCEs. So, one of the ways to control the above said SCEs is by using more than two gates and a lean fully depleted (FD) semiconductor body. The predictions of International Technology Roadmap for Semiconductors (ITRS) are followed by the device designers to propose various novel device structures and process parameter variations[13]. Again UTB double gate (DG) MOSFET can be scaled more intrusively than bulk Si schema . A double gate structure fabricated on SOI wafer has been employed in CMOS technology because of its outstanding SCEs immunity, high current drivability (Ion) and lower leakage current (Ioff) as compared to the bulk MOSFETs[**?**].

3.2 Simulation

The schematic diagram of the UT-SDOI single gate (SG) and double-gate (DG) MOSFET structures are used for modeling and simulation as shown in Figure 3.1. The buried oxide thickness, gate oxide thickness and the silicon are tb = 40 nm, tox= 0.9 nm and tSi= 5 nm, respectively.
The gate length L_g= 20 nm, with under lap L_{un}=5 nm considered towards both side of channel. The source drain length fixed at L_{sd}=40 nm. For all devices, the work function of the gate metal is defined between M = 4.6 eV to 4.7 eV to achieve a constant leakage current I_{off} =0.15 nA. The device has uniformly doped sourcedrain with doping concentration of $N_D = 1 \times 10^{20} cm^{-3}$. The channel is kept lightly doped with doping concentration of $N_A = 1 \times 10^{15} cm^{-3}$ The simulation is carried out by the device simulator Sentaurus, a 2-D and 3-D numerical simulator from Synopsis Inc. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation.. All the structure junctions are supposed to be abrupt, and the biasing conditions pondered at 250C in the simulation[14].

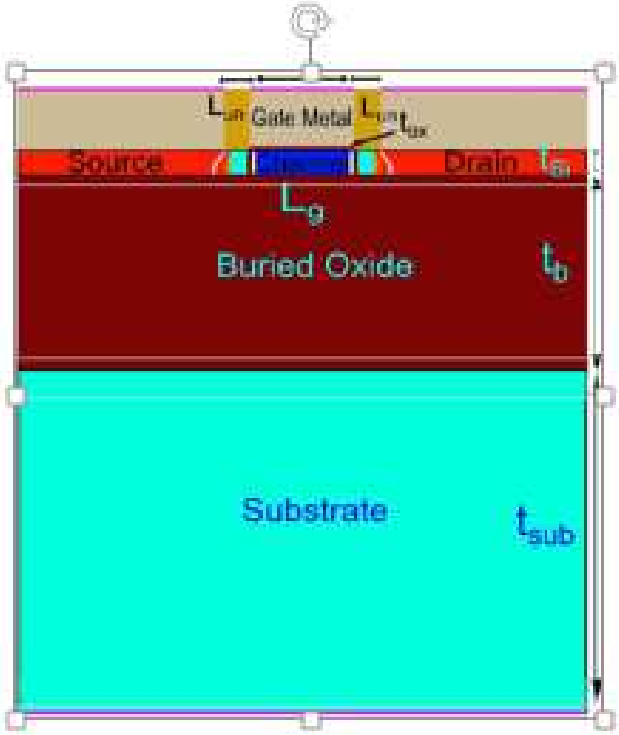

Figure 3.1: Schematic Structure of UT-SG SDOI

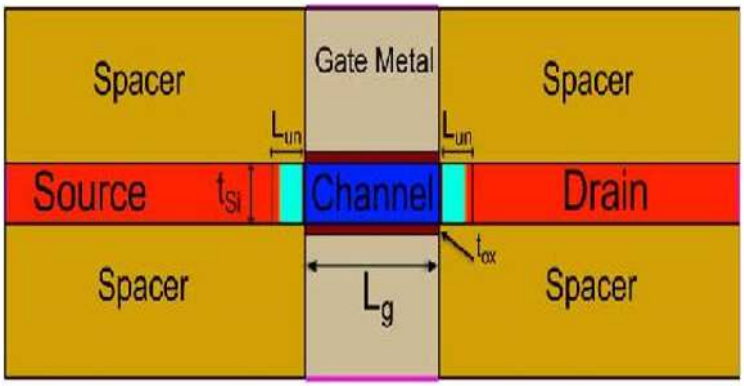

Figure 3.2: Double Gate SDOI MOSFET

3.3 Result and Discussion

3.3.1 Doping profile for SG and DG PMOS and NMOS

To study the potential along the channel we have taken the cutline in the center of the channel thickness across the channel of the devices. The drift-diffusion model is the default carrier transport model in Sentarous device is activated. The basic mobility model is used, that ponder the effect of high-field saturation (velocity

saturation), doping dependence, and transverse field dependence. The impact ionization effects are ignored. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated. An iterative approach is followed to solve the device equations. The iteration continues, till it attains a small enough error limit[15].

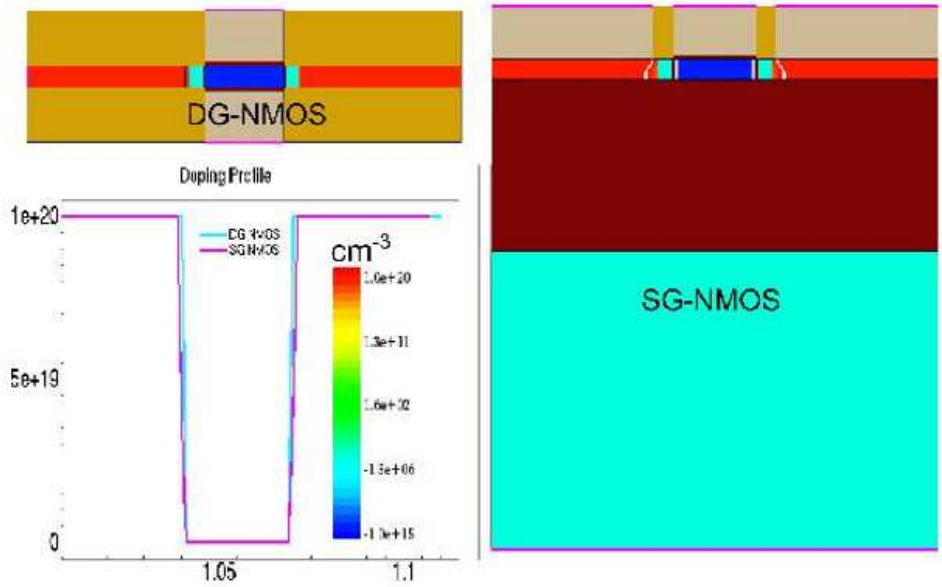

Figure 3.3: Doping profile of the UT-SDOI MOSFET structures for SG and DG NMOS

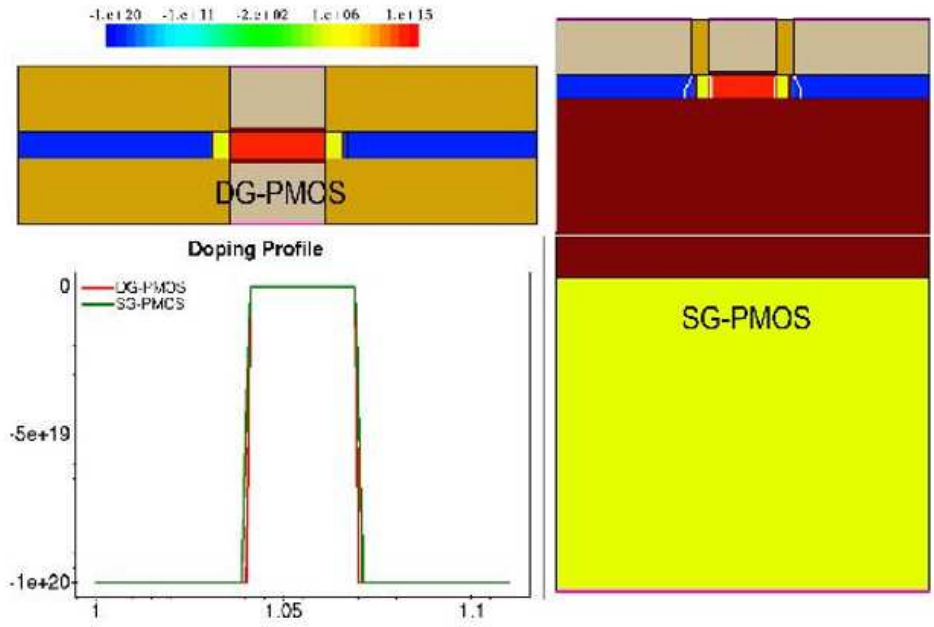

Figure 3.4: Doping profile of the UT-SDOI MOSFET structures for SG and DG PMOS

The doping profile for both nmos and pmos are demonstrated in Figure 3.3 and Figure 3.4. The simulation is carried out by the device simulator Sentaurus, a 2-D and 3-D numerical simulator from Synopsis Inc.

3.3.2 ID-VGS characteristics for SG and DG SDOI MOSFETs

The ID-VGS characteristics of a CMOS with 5 nm body portliness and 20 nm gate lengths are shown in Figure 3.5. As shown in the figure, the ID-VGS have matched Ioff and Vth as centred for both NMOS and PMOS devices, which are achieved by tuning the metal gate work function. Also by observing the Figure 3.5, having constant Ioff, the UT -SDOI DG shows a higher drive current than its counterpart UT-SDOI SG. Typical output characteristics of both NMOS and PMOS, UT-SDOI SG and DG devices are demonstrated in Figure 3.6 and report as a fully functional and long channel behaviour. Furthermore, one can clearly say that these devices are fully depleted (FD) as there is no kink effect. Because of high electron mobility, the NMOS shows a higher current than PMOS. Again by comparing between UT-SDOI SG and DG devices, the DG configuration depicts a 30

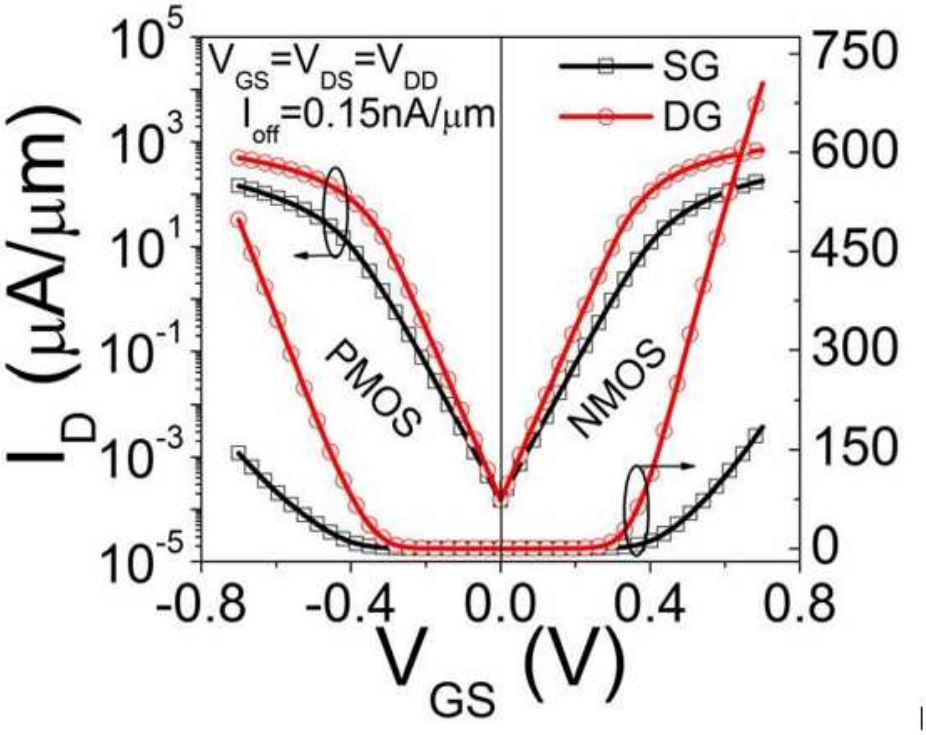

Figure 3.5: The characteristics of both UT-SDOI SG and DG MOSFETs (n and p type) for the transfer curve between drain current (ID) and gate voltage

The channel potential distributions for both NMOS and PMOS, UT-SDOI SG and DG devices are demonstrated in Figure 3.7 and Figure 3.8 respectively. The inset figures represent field distribution of devices. From the graph, the potential barrier height of DG is little lower than SG which leads to a lower threshold voltage for DG MOSFETs. A lower threshold voltage with acceptable SCEs is very much useful for high performance (HP) applications according to ITRS-2011. So a double-gate ultra- thin body i.e.tsi =5nm MOSFET is a good candidate for HP applications.
The above figures illustrates the on-off ratio for both NMOS and PMOS, UT-SDOI SG and DG devices. SDOI DG devices endow more on current than SG device, emerging in a rapid switching time. It can be measured from the figure that for SDOI DG, on-off ratio increases around a factor of 4 than SDOI SG in case of NMOS and a factor of 3 in case of PMOS. SG devices have several leakage mechanisms like band-to-band- However, DG devices have two major leakage mechanisms as subthreshold leakage and gate leakage tunnelling (BTBT), gate induced drain leakage (GIDL), sub threshold leakage, gate leakage, and reverse bias junction. However, DG devices have two major leakage mechanisms as subthreshold leakage and gate leakage. The increase of drain current of SDOI DG is because of the lack in parasitic source-drain resistances.

The drain induced barrier lowering (DIBL) and threshold voltage are compared between UT-SDOI SG and

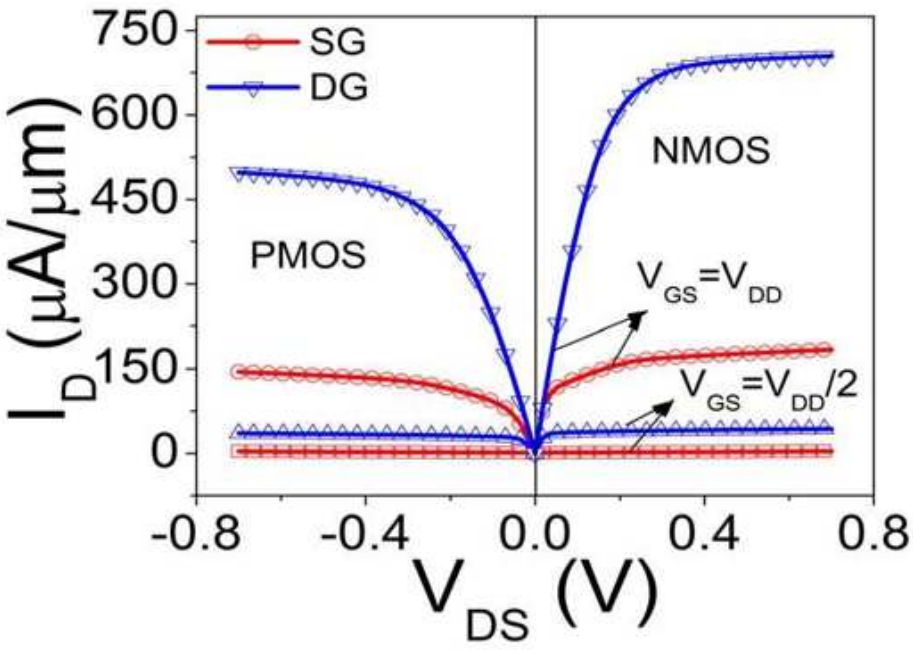

Figure 3.6: The characteristics of both UT-SDOI SG and DG MOSFETs (n and p type) for the output curve between drain current (ID) and drain voltage

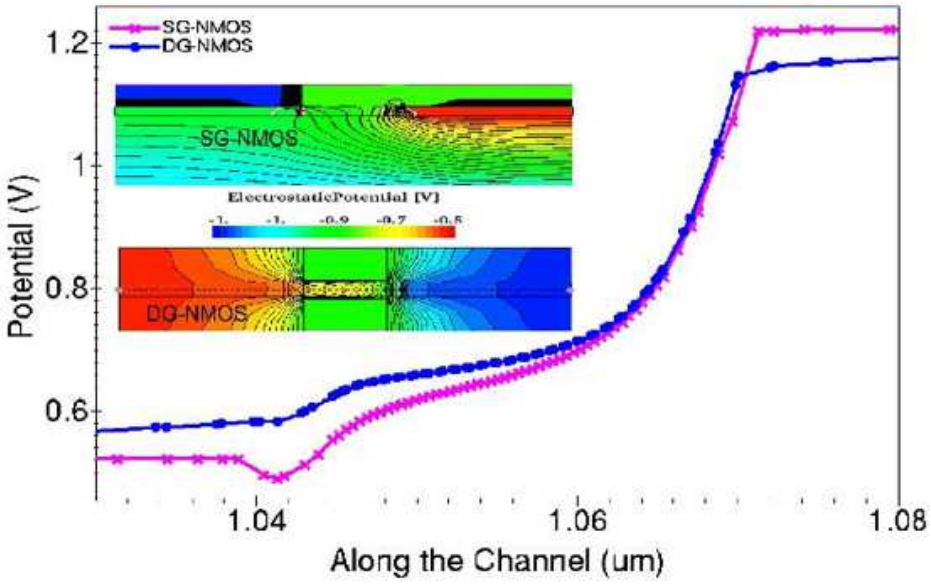

Figure 3.7: Potential variation along the channel length at $V_GS = V_DS = 0.7$V for UT-SDOI SG and DG MOSFET NMOS devices

DG MOSFET in Figure 3.10 and Figure 3.11. As thinner body thickness (tSi), and number gates are more in case of UT-SDOI DG, owing a low value of natural length λ which is desirable to minimize the SCEs. So, the Vth is less sensitive to VDD in case of UT-SDOI DG MOSFET than its SG counterpart, further leads to a less DIBL effect.

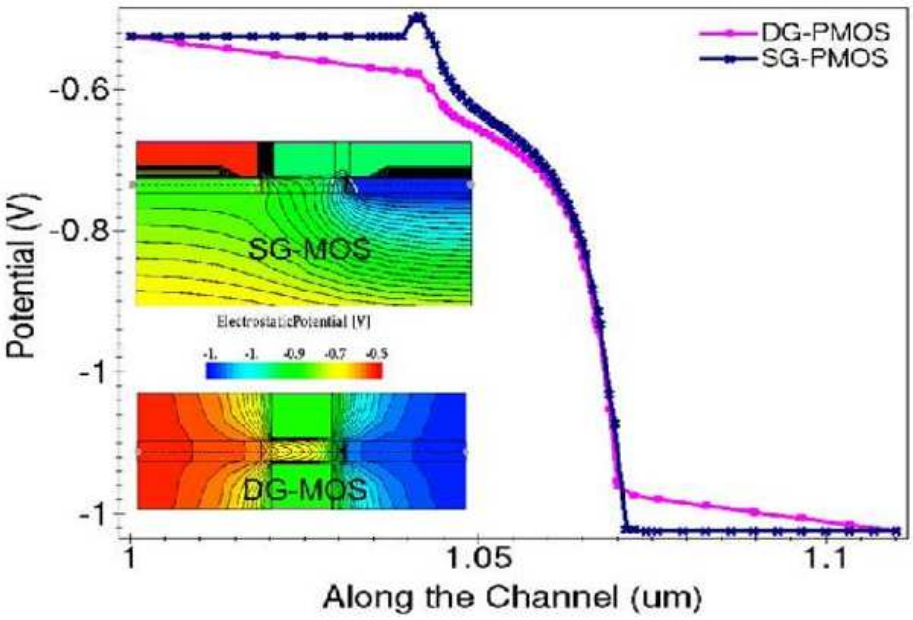

Figure 3.8: Potential variation along the channel length at $V_GS = V_DS = 0.7$V for UT-SDOI SG and DG MOSFET PMOS devices

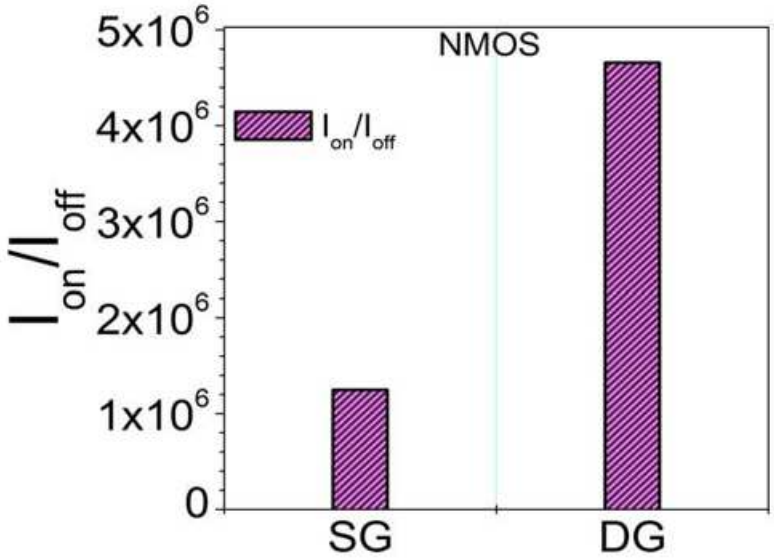

Figure 3.9: Ion/Ioff ratio of UT-SDOI SG and DG MOSFET NMOS devices

3.3.3 Summary

t In this case,the sensitivity and trend of Vth, Ion/Ioff ratio and potential of UT-SDOI SG and DG MOSFET for both P-type and N-type cases are established through proper simulation setup. The device dimensions

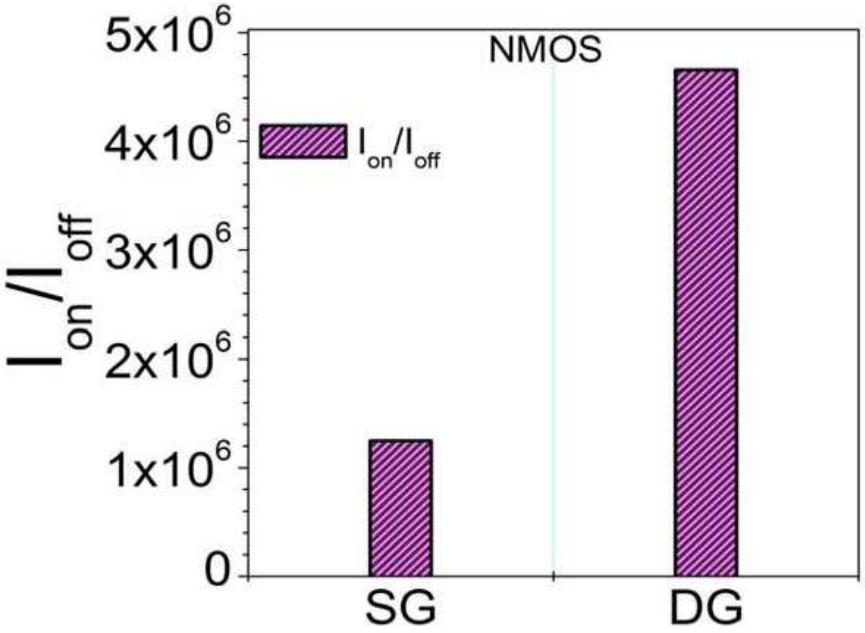

Figure 3.10: Ion/Ioff ratio of UT-SDOI SG and DG MOSFET PMOS devices

are considered in the work are according to ITRS-2011 roadmap. The designs are valid for all three types of applications like high performance (HP), low operating power (LOP), and low standby power (LSTP). From the results, the UT-SDOI DG shows a higher drive current and lower DIBL than its counterpart UT-SDOI SG even maintaining a constant Ioff. The on-off current ratio for SDOI DG increases around a factor of 4 than SDOI SG in case of NMOS and a factor of 3 in case of PMOS case.From all analysis UT-SDOI DG MOSFET has potential to meet the ITRS roadmap for 22nm technology node and below this node with considerable amount of design flexibility for HP and LOP devices are achievable. However, LSTP design specification may be feasible by considering a scaled version of oxide thickness.

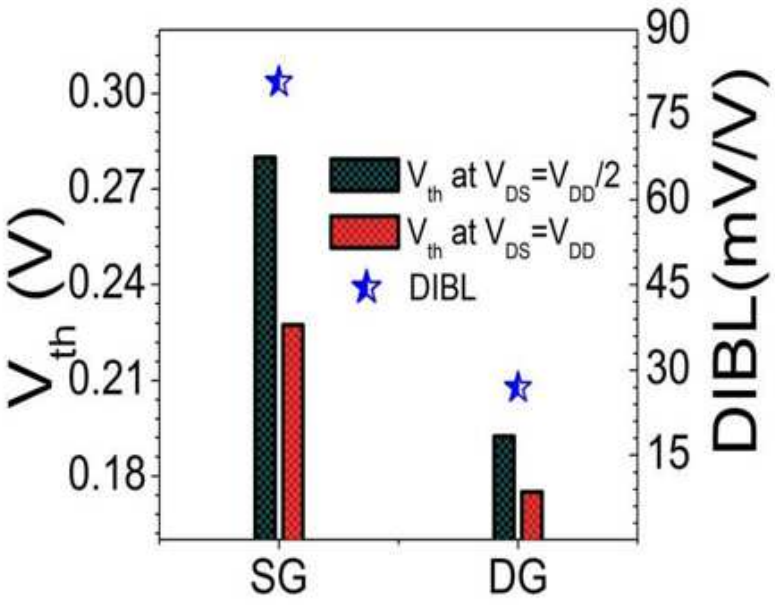

Figure 3.11: Two important short channel effects threshold voltage (Vth) variation and drain induced barrier lowering (DIBL) of UT-SDOI SG and DG MOSFET (a) NMOS devices

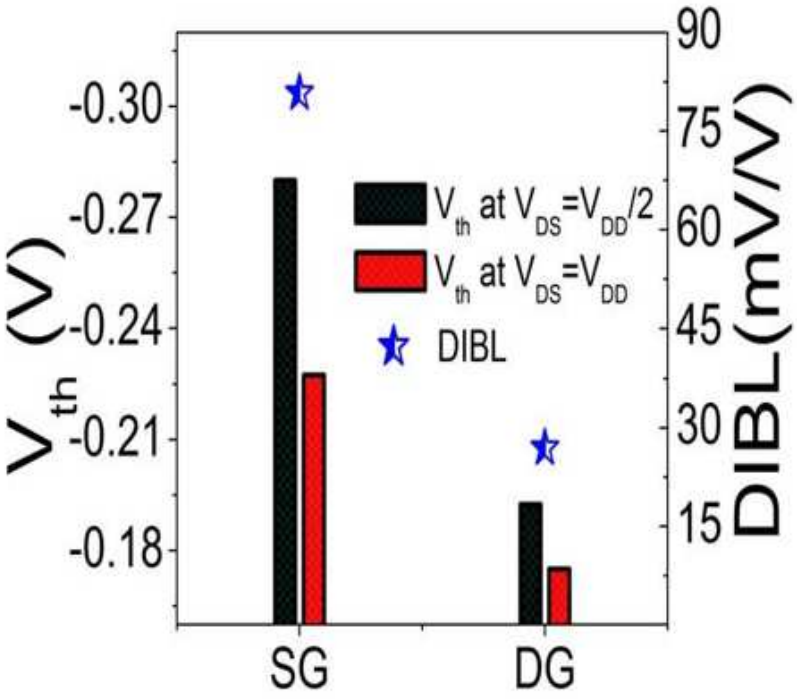

Figure 3.12: Two important short channel effects threshold voltage (Vth) variation and drain induced barrier lowering (DIBL) of UT-SDOI SG and DG MOSFET (b)PMOS devices

Chapter 4

Investigation of UTB-SG and III-V DG MOSFETs with Channel Engineering

4.1 Introduction

For high density integrated circuits such as microprocessors and semiconductor memories, most important device used is metal-oxide-semiconductor- field-effect transistor (MOSFET). The principle proposed by Lilienfeld and Heil , with subsequently the first MOSFET reported by Kahng and Atalla in 1960[16] . The integrated circuit processing techniques have led to continuing reduction in both horizontal and vertical dimensions of the devices. Both the performance and density of the devices have grown exponentially with the shrink of technological channel length and fabrication cost. Due to their extremely small sizes, those devices are used for ultra-high density integrated electronic components having billions of devices in a single chip[17] . Many investigations have been done for multi-gate devices to comply with static electrical figures of merit (FoMs) such as Ion/Ioffratio, drain induced barrier lowering (DIBL),subthreshold slope (SS) etc. as per requirements of ITRS for logic operation[18] .
Ultra-thin-body (UTB) MOSFETs are attractive candidates for nanoscale device at the end of ITRS as they exhibit better electrostatic integrity (E.I.).Non classical silicon MOS structures such as FinFETs in 3-D, DG-MOSFET in 2-D, are replacing the conventional bulk MOS devices because of their capability to attain higher speeds and reduced short channel effects (SCEs) with the added advantage to design highly integrated CMOS circuits and better analog/RF applications[19].

4.2 Device design

4.3 Simulation

The technology parameters and the supply voltages used for the device simulations are according to the analog ITRS roadmap for below 50 nm gate length devices. The VDD is taken as 0.7V. The work functions of the metal gates are fixed at 4.5eV to achieve the desired Vth value. The drift-diffusion model is the default carrier transport model in Sentaurus device simulator, which is activated in the simulation[5]. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation[20].

Design	HP	LOP	LSTP	This Work	
				UTB SG-MOS	UTB DG-MOS
Lg(nm)	20	20	20	100 nm to 20 nm	
EOT (nm), tox	0.84	0.9	1.2	0.9 nm	
VDD(V)	0.85	0.67	0.87	0.7 V	

Table 4.1: DEVICE PARAMETERS USED IN THETCADSIMULATION OBTAINED FROM ITRS 2013

4.4 Result and Discussion

Variation of Channel Length and Doping Concentration

The simulated I_D-V_{GS} characteristics for both SG and DG devices are shown in the figure for different channel lengths at low (50 mV) drain bias. Making a comparison among Figure 5.2 and Figure 5.3, it can be observed that with similar channel lengths, DG device has superior performance as compare to SG because of low leakage current. While considering $L_g = 20nm$ case for both devices, SG provides a leakage current of 10-6 A/micrometer whereas DG gives a reasonable leakage current i.e. in the range of 10-8 A/micrometer.
The above Figure demonstrates the ID-VGS characteristics of 40 nm UTB-DG MOSFET at low bias of VDS=50 mV for different doping profiles. The effect of doping profile variations on drain current is studied by considering four different cases. In profiles (iii) and (iv) i.e.$N_A = 1 \times 10^{17} cm^{-3}$ and $N_D = 1 \times 10^{18} cm^{-3}$ cm-3 respectively, the DG configuration shows a low Ion as compare to profiles (i) and (ii) i.e. NA=1x1015 cm-3 and NA=1x1016 cm-3 respectively. This is because of the mobility degradation in case of heavily doped channel i.e. cases (iii) and (iv).
Again similar analysis are carried out as previously discussed in the above figures at a higher drain bias of $V_{DS} = 0.7V$ to study the effect of VDS on device performance. From Figure 5.6 and Figure 5.7, the Ioff is very low in terms of 10^{-7} A/micrometer in case of DG as compare to SG (Ioff in terms of 10^{-4} A/micrometer). So, VDS has a less influence on DG configuration as compare to SG which further decreases the drain induced barrier lowering (DIBL) effect.
The Figure describes the Lg dependence of DIBL and Ion/Ioff ratio for both UTB SG and DG devices. The DIBL increases as the channel length decreases due to the Vth roll off effect in shorter Lg., the DIBL is very low in case of DG as compare to SG shown in Figure 5.8. This is because of the less influence of VDS on DG configurations as already discussed. So, it identifies that the electrostatic control of gate is more in case of DG device. The on-off ratio (Ion/Ioff) is also discussed for both devices with different Lg. DG configuration shows a 13
Figure 4.9 shows the percentage of Ion/Ioff ratio for UTB- DG MOSFET with different doping profiles. For low stand by power applications (LSTP), this ratio has a significant impact and higher value of this ratio is desirable. From Figure 4.9, Ion/I offratio increases in accordance with the doping concentrations.
This is because higher doping concentration is required to control the threshold voltage and minimize the short channel effects which further decreases the leakage current. So, a maximum 43.1 percentage Ion/Ioff ratio can be achievable in case of doping profile of NA=10 18 cm-3. The subthreshold slope (SS) variation with Lg for both the devices at two different drain biases (VDS=50 mV, and 0.7 V) is plotted in Fig. 4(c). SS can be calculated as SS= VG/ (log ID) and the typical value is 60 mV/decade as marked in Figure 5.10. As per the result, for higher Lg(100 nm, 80 nm, and 60 nm) the SS shows approximatelyideal value for both device cases. However, as Lg decreases (40 nm, and 20 nm) the SG configuration demonstrates a higher SS value as compare to DG. This is because SG configuration is more prominent towards SCEs for lower Lg and the gate loses its control over channel. Similarly Figure 5.11 shows the SS values for DG device at different doping profiles. Lower doping profiles give a better SS value for DG configuration and increases with doping concentrations.

4.4.1 Effect of High Mobility Channel Materials

It is widely anticipated that strained silicon may run out of steam and alternative channel materials will be required to instate the targets set out by ITRS[5]. While several grand challenges must be chasten to realize III-V N-MOSFETs incorporation in future C-MOSFETs. High mobility (low-bandgap) materials like GaAs, In0.53Ga0.47As which are the combination of elements of III and V columns of periodic tableshow a significant amount of augmentation in on current but endure from the BTBT leakage current i.e. off current. These materials are the alternatives to reach to the predicted performance of the CMOS technology.
Figure shows that drain current is maximum for the InGaAs due to its high mobility at VDS=50 mV and can be used for the switching applications. The drain current of the saturation region i.e. at $V_{DS} = 0.7V$ is shown in the Figure. But the static power dissipation is more in high mobility materials due to the high leakage currents as shown in Fig. 5(c) which can be compensated with the high drain current particularly for the switching applications.
All the above discussed parameters are extracted for both devices and tabulated in Table III, IV and V. By comparing the data from both tables, we can say the UTB-DG configuration shows a better results in terms

Material Parameters	Si	GaAs	In0.53Ga0.47As
EG (eV)	1.12	1.424	0.751
r	11.7	12.9	13.9
(cm2V-1s-1)	200	500	1300
ni (cm-3)	1.15x1010	2.15x106	6.37x1011

Table 4.2: Material parameters used in DG-MOSFET for the simulation

DG-MOS	Threshold,Voltage,Vth(V)		DIBL	Ion, (A)	Ioff, (A),VGS=0V	SS (mV/decade)	
Lg	VDS=0.05 V	VDS=0.7 V		VDS= VGS,=0.7V	VDS=0.7V	VDS=0.05V	VDS=0.7V
100	0.19	0.18	8	5.80x10-4	7.77x10-11	60.08	59.92
80	0.19	0.18	19	6.38x10-4	9.97x10-11	60.23	60.05
60	0.17	0.16	23	7.11x10-4	1.46x10-10	60.61	60.61
40	0.17	0.15	27	8.24x10-4	4.41x10-10	60.42	62.65
20	0.07	0.01	92	1.03x10-3	1.49x10-7	62.78	-

Table 4.3: Static electrical FOMS for DG-MOSFET

of SS, DIBL, and Ioff.

4.4.2 Summary

Here a UTB-SG and DG-MOSFET have been simulated. After designing of these two MOSFETs we draw the layout and simulate the parameters available in these MOSFETs. The different electrostatic parameters have been systematically represented for both the MOSFETs by varying Lgand channel doping (N A). From the results, the UTB-DGMOSFET shows an improvement in device performance in terms of SS, DIBL and on-off ratio (Ion/Ioff) over the SG-MOSFET. With the use of high mobility channel materials (GaAs, In0.53Ga0.47As) in DG MOSFET, we have found that a strong decrease of DIBL in GaAs and In0.53Ga0.47As. Our result shows that In0.53Ga0.47As based DG MOSFETs have the lower DIBL, but is the most impacted by quantum confinement effects. So by comparing these parameters, DG MOSFET with high mobility materials exhibits high drive current which is more suitable for better switching application.

DG-MOS	Threshold,Voltage,Vth(V)		DIBL	Ion, (A)	Ioff, (A),VGS=0V	SS (mV/decade)	
Lg	VDS=0.05 V	VDS=0.7 V		VGS,=0.7V	VDS=0.7V	VDS=0.05V	VDS=0.7V
Si	0.070	0.010	92	1.03x10-3	1.49x10-7	62.78	-
GaAs	0.285	0.25	53.84	1.16x10-3	2.91x10-7	79.18	79.042
In0.53Ga0.47As	0.281	0.251	46.15	1.41x10-3	3.79x10-7	78.98	78.84

Table 4.4: PERFORMANCE COMPARISON OF DG-MOSFET BY CONSIDERING DIFFERENT CHANNEL MATERIALS

SG-MOS	Threshold,Voltage,Vth(V)		DIBL	Ion, (A)	Ioff, (A),VGS=0V	SS (mV/decade)	
Lg	VDS=0.05 V	VDS=0.7 V		VDS= VGS=0.7 V	VDS=0.7V	VDS=0.05V	VDS=0.7V
100	0.19	0.18	15	3.25x10-4	1.49x10-10	64.96	63.67
80	0.19	0.17	27	3.63x10-4	2.83x10-10	65.03	65.54
60	0.17	0.14	54	4.23x10-4	1.19x10-9	68.89	70.42
40	0.12	0.03	135	5.25x10-4	4.20x10-8	82.35	-
20	-	-	-	7.62x10-4	5.15x10-5	-	-

Table 4.5: Static electrical FOMS For SG-MOSFET

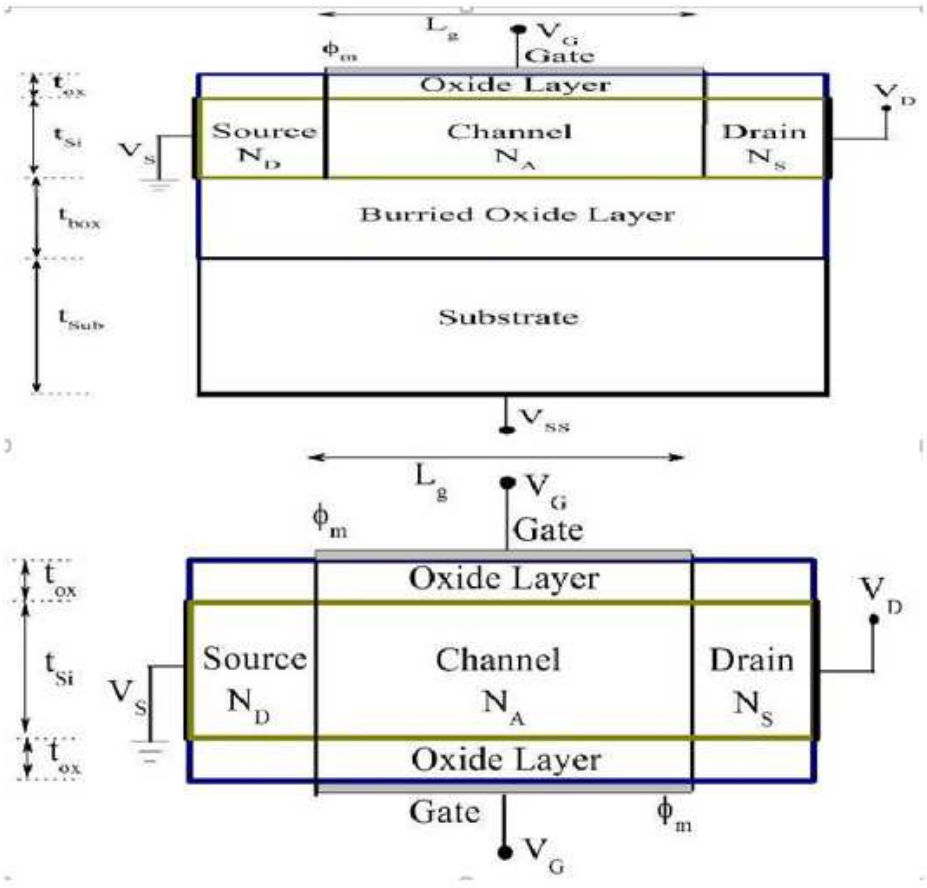

Figure 4.1: 2-dimenssional cross sectional view of the (a) UTB SG-MOSFET (b)UTB DG-MOSFET

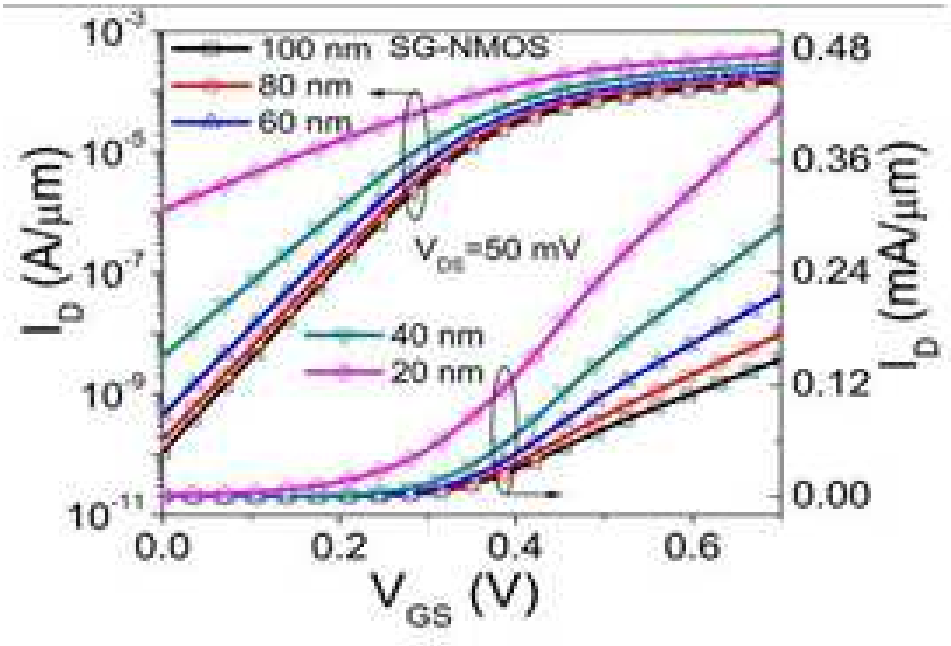

Figure 4.2: Drain current (ID) of the devices as a function of gate to source voltage for $V_{DS} = 0.05V$ (a) SG with variation of L_g

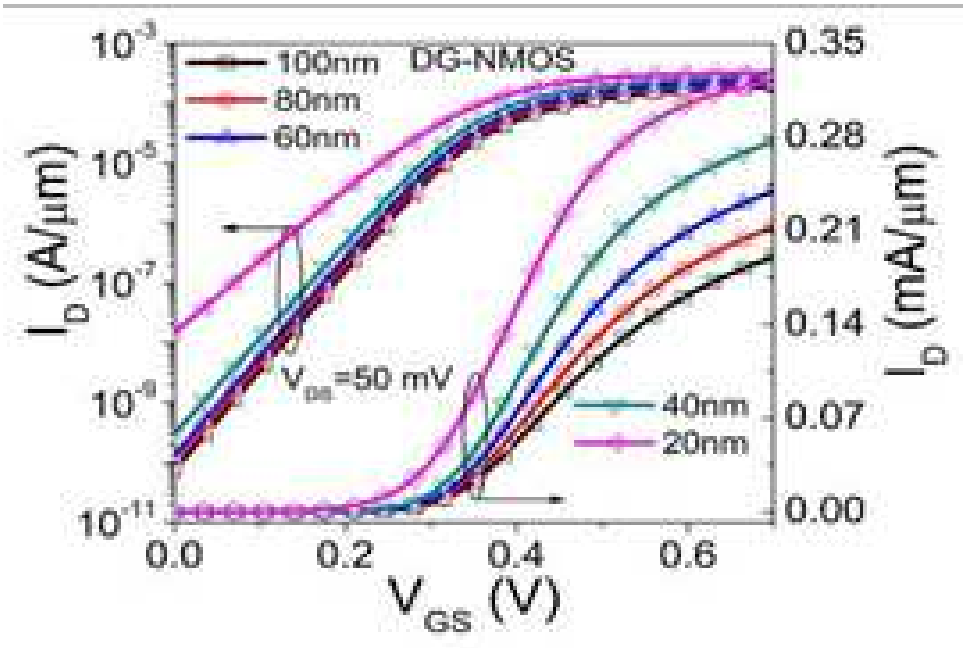

Figure 4.3: Drain current (ID) of the devices as a function of gate to source voltage for $V_{DS} = 0.05V$ (b) DG with variation of L_g

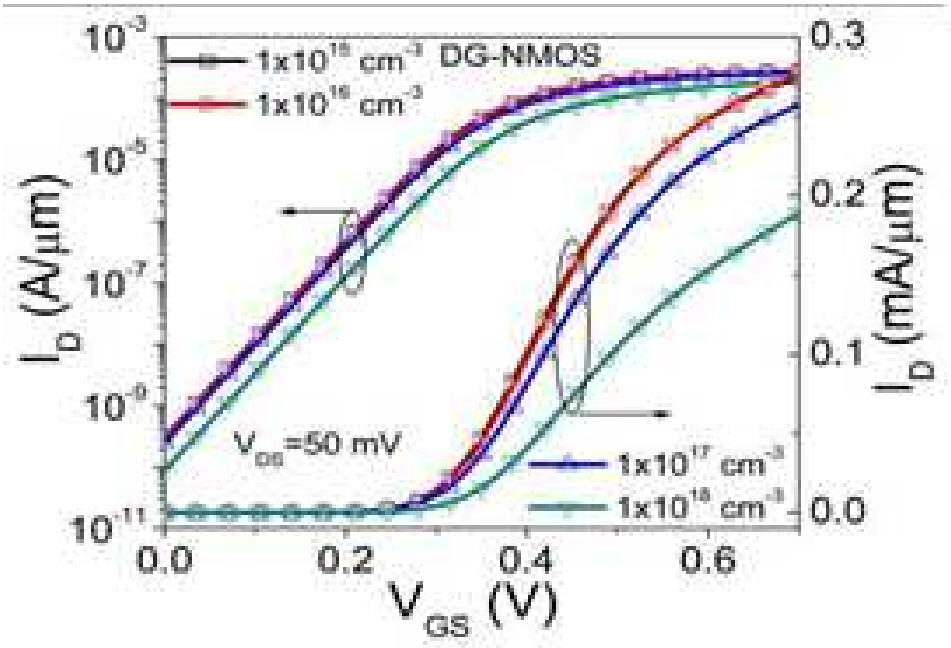

Figure 4.4: Drain current (ID) of the devices as a function of gate to source voltage for $V_{DS} = 0.05V$ of DG for different N_A

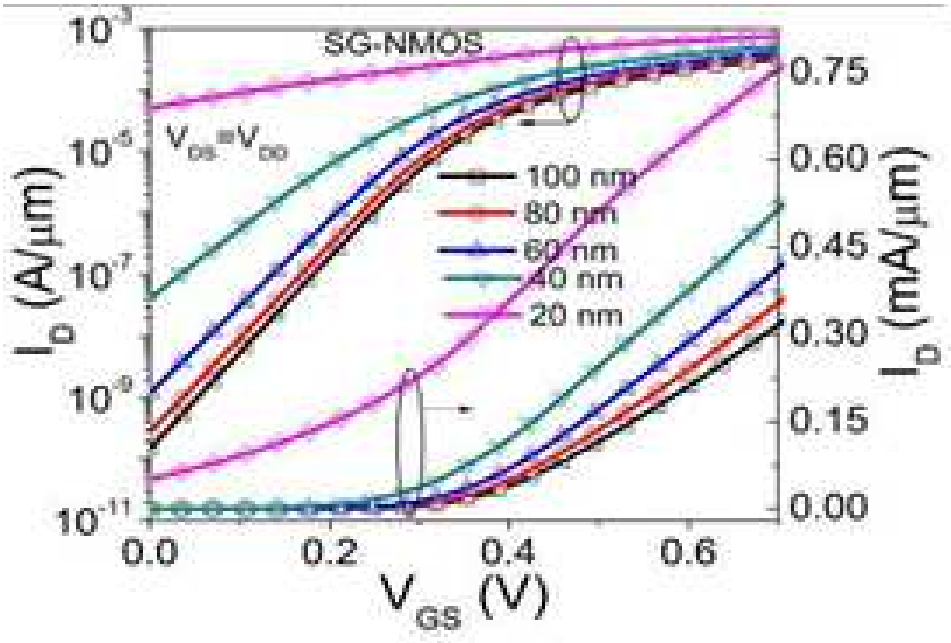

Figure 4.5: Drain current (ID) of the devices as a function of gate to source voltage for $V_{DS} = 0.07V$ (a)SG with variation of L_g

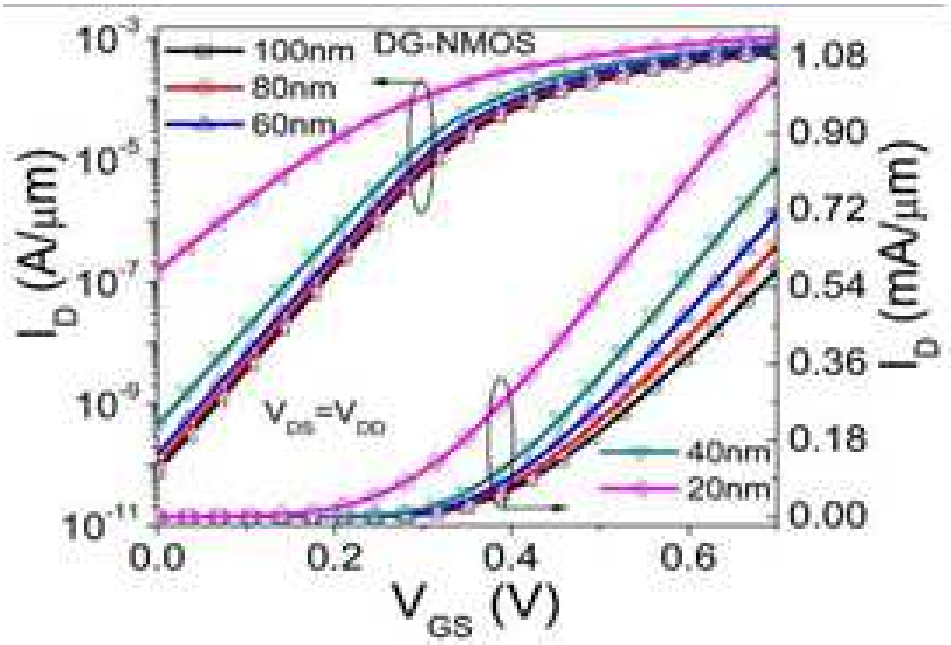

Figure 4.6: Drain current (ID) of the devices as a function of gate to source voltage for $V_{DS} = 0.07V$ (b)DG with variation of L_g

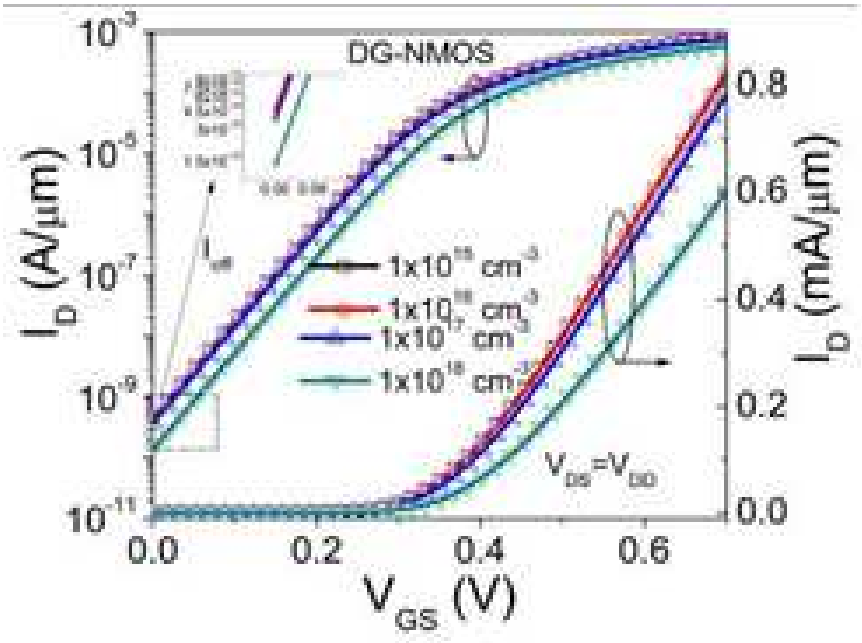

Figure 4.7: Drain current (ID) of the devices as a function of gate to source voltage for $V_{DS} = 0.07V$ (c)DG with variation of N_A

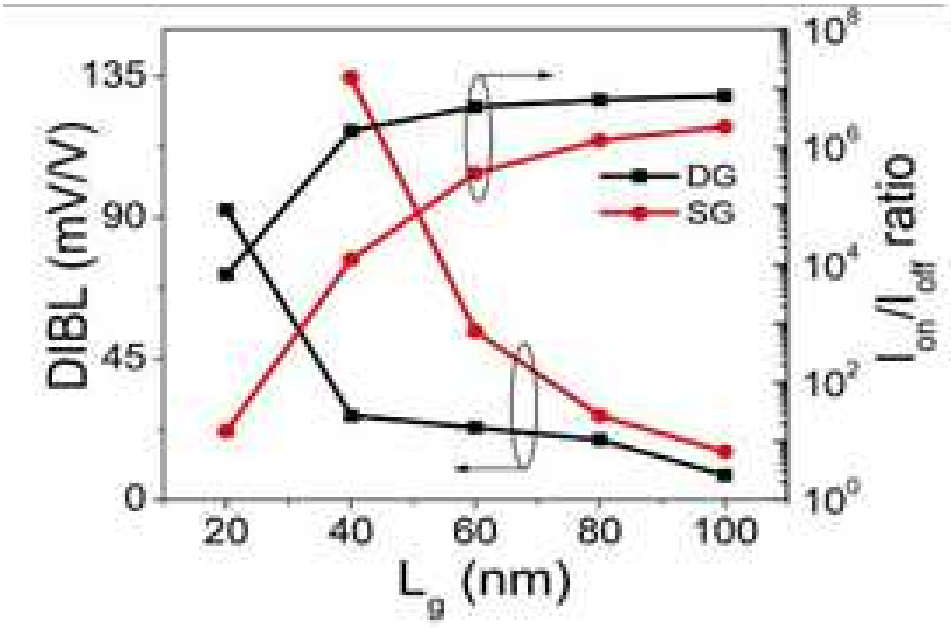

Figure 4.8: The performance metrices for both SG and DG MOSFETs at $V_{DS} = 0.05V and 0.7V$(a) DIBL and Ion/ Ioff ratio for different L_g

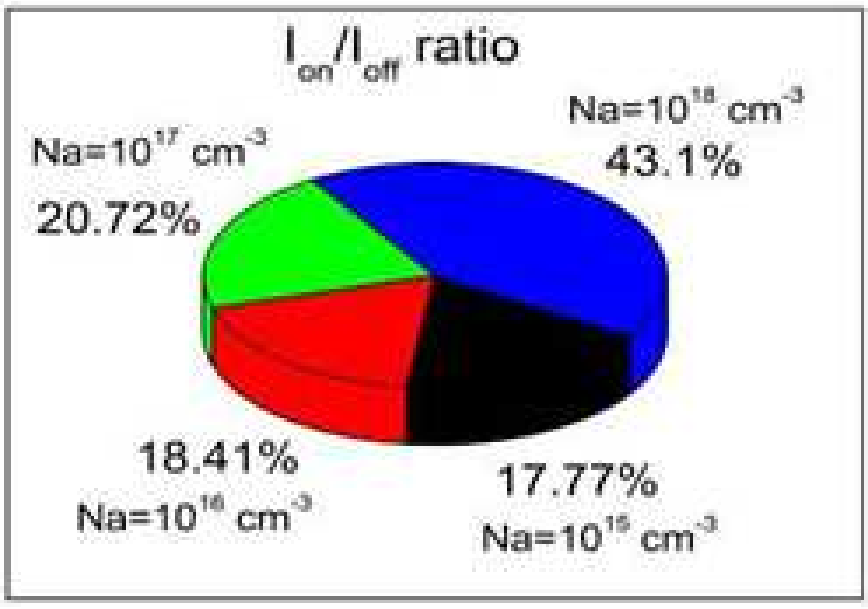

Figure 4.9: The performance metrices for both SG and DG MOSFETs at $V_{DS} = 0.05V and 0.7V$(b) Ion/Ioffratio of DG with variation of N_A

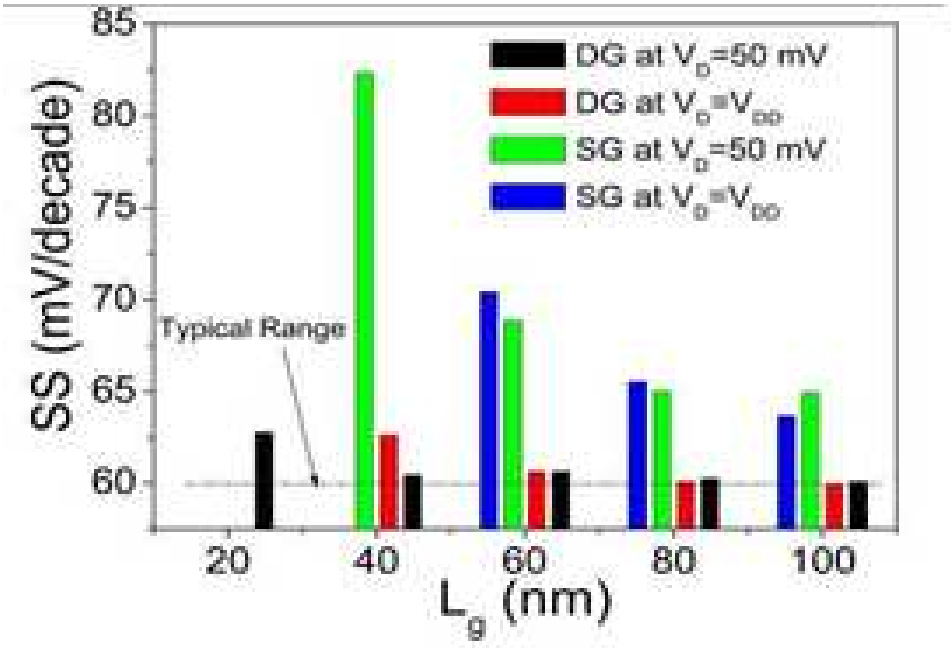

Figure 4.10: The performance metrices for both SG and DG MOSFETs at $V_{DS} = 0.05V and 0.7V$(c) SS for different L_g

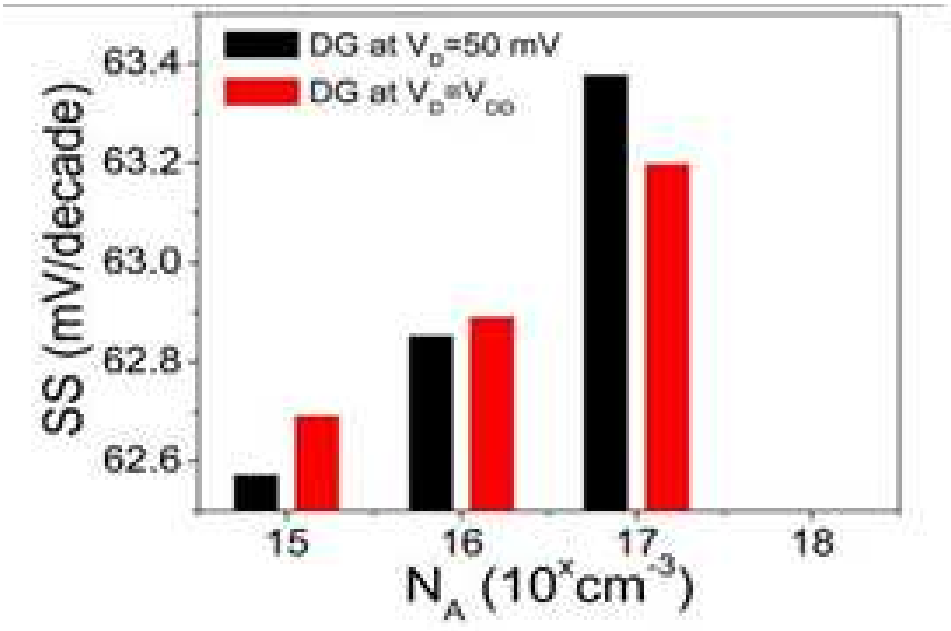

Figure 4.11: The performance metrices for both SG and DG MOSFETs at $V_{DS} = 0.05V and 0.7V$(d) SS with variation of N_A

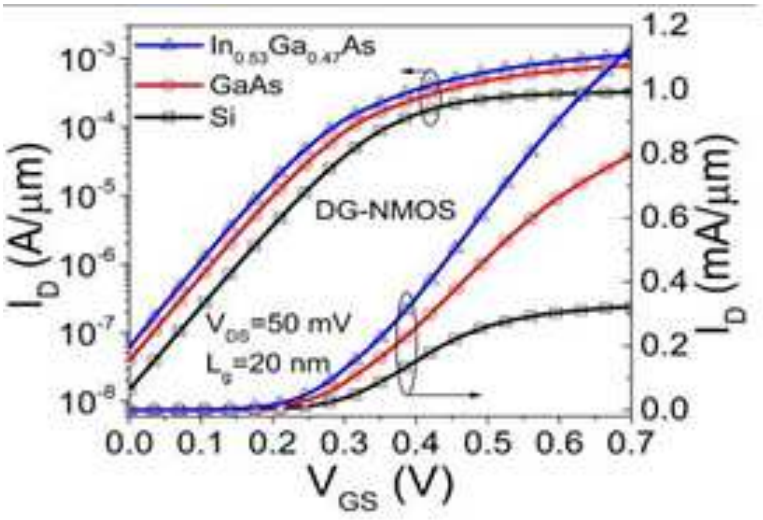

Figure 4.12: Effects of high mobility channel materials for DG MOSFET at $V_{DS} = 0.05Vand0.7V$ using different materials of Drain current variation for the linear region

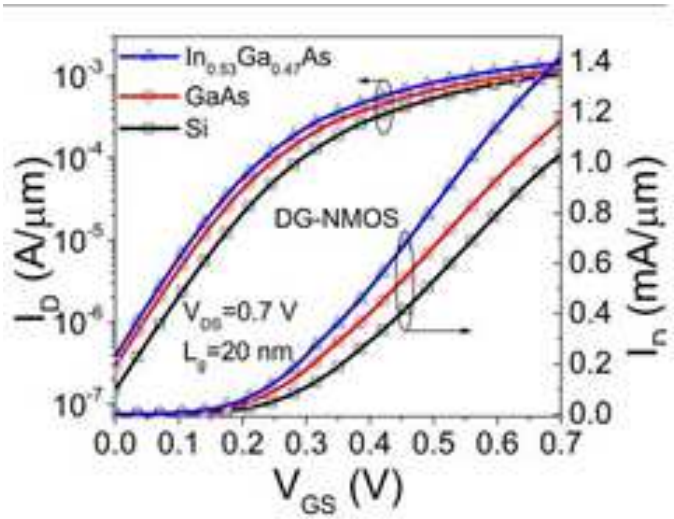

Figure 4.13: Effects of high mobility channel materials for DG MOSFET at $V_{DS} = 0.05Vand0.7V$ using different materials of Drain current variation for saturation region

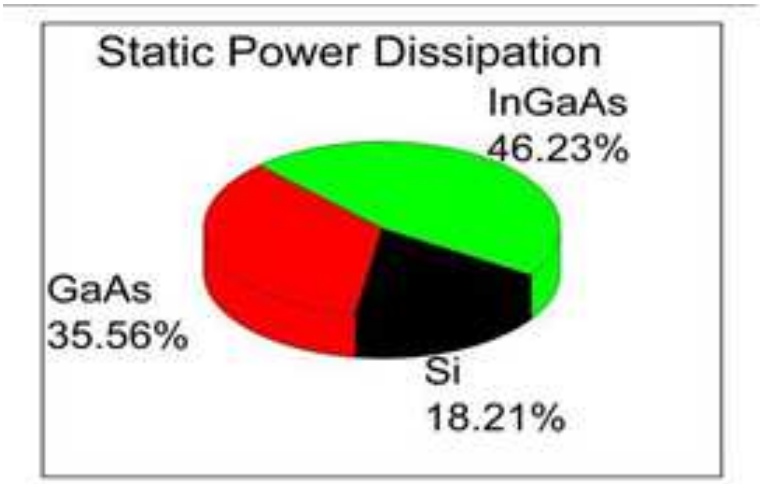

Figure 4.14: Effects of high mobility channel materials for DG MOSFET at $V_{DS} = 0.05V and 0.7V$ using different materials (c)Static power dissipation pie chart

Chapter 5

Performance analysis between UTB-SG and DG-MOSFETs with and without presence of noise

5.1 Introduction

Several theoretical, process and physics-based analysis have been linked to short channel effects which is observed on the DC properties of the devices, the limitation or degradation of the high frequency and noise characteristics along the down-scaling of the channel length has not been described widely .Here the Small signal and RF noise properties of up-to-date and up- coming SOI MOSFETs will be discussed at the theoretical point of view. Here we present an analytical method for RF and noise modeling including short channel effects[15]. In the first section, DC Characteristic of noise model is presented for both Single gate and Double gate MOSFET. In the second section, comparative study between Single gate and Double gate MOSFET has been done with the addition of noise. The present work described the comparative study of noise in single gate and double gate Nano scale SOI MOSFETs for radio frequency applications, such as a low noise amplifier, power amplifier and modulator.Here we have investigated the performance comparison between SG and DG MOSFET with and without presence of noise[21].

5.2 Device design

Planar symmetric UTBDG-MOSFET has been considered whose schematic structure is shown in Figure1. An SOI MOSFET requires film thickness just one fourth of the channel length (Lg) for better control of transistor.Source and drain extensions are 60nm long from the edges of the gates, with metal contacts vertically placed at their ends. The body thickness(TSi) of the device is varied from 50nm to 150nm.All the structure junctions are assumed as abrupt.Both SG and DG-MOSFET operate with power supply voltage VDD=0.7V.

5.3 Simulation

The simulated devices consist of UTB-SG and DG-MOSFET operating with a power supply voltage of VDD=0.7V. Source/channel and channel/drain junctions are assumed to be abrupt with continuous doping of $N_D = 1 \times 10^{20} cm^{-3}$ cm-3 in Source/Drain regions. Different ID-VG characteristics has been done at different drain to source voltage i.e. at VDS=0.05V and 0.7V respectively. The main differences between both structures arise when comparing the induced fluctuations in the gate current: the fluctuations are consistently higher in the double gate structure. The work functions of the metal gates are fixed at 4.5eV to achieve the desired Vth value. The drift-diffusion model is the default carrier transport model in Sentaurus device simulator, which is activated in the simulation[22]. In addition the basic mobility model is used to consider the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored in our device simulation. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation.

5.4 Result and Discussion

5.4.1 Transfer Characteristics for SG-MOSFET with and without noise

The simulated ID-VGS characteristics for both SG with and without noise are shown in the following figures at low (50 mV) drain bias. Making a comparison among the figures , it can be observed that, SG device without noise has superior performance as compare to SG device with noise because of low leakage current.

Table 5.1: Statistical electrical FoMs for SG-NMOS with and without presence of Thermal noise VDS=0.05V and 0.7V

SG-NMOS	Threshold Voltage, Vth,VDS=0.05V, VDS=0.7V		DIBL	Ion(A), VDS=VGS=0.7V	Ioff(A), VGS=0V VDS=0.7V	SS(mV/Decade) VDS=0.05V VDS=0.7V	
Without Noise	0.3675	0.3325	53	0.00025	5.00E-11	73.378	75.089
With Noise	0.2275	0.1575	107	0.0004	1.21E-08	73.327	-

From the figure 5.6 and 5.7 it is observed that SG-NMOS with noise shows a leakage current 10^{-8}A/micrometer whereas SG without noise shows a leakage current in terms of 10^{-9}A/micrometer .Hence SG-NMOS device device without presence of thermal noise has superior performance as compare to SG device with presence of thermal noise because of low leakage current.It is also seen that Ioff is low in SG NMOS without noise as compare to SG NMOS with noise.

5.4.2 DIBL and Ion/Ioff ratio for SG MOS with and without noise

If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL).The DIBL increases as the body thickness decreases due to V_{th} roll off effect.Mathematically, $DIBL = (V_{th1}\text{-}V_{th2}/V_{DS2}\text{-}V_{DS1})$
From the above figure it is observed that Ion/Ioff ratio increases for SG MOS without noise as compare to SG MOS with presence of thermal noise.DIBL is low in case of SG-MOSFET without noise (in terms of 53 mV/V)as compare to SG with presence of thermal noise(in terms of 107mV/V). This is because of the less influence of VDS on SG without noise configurations.

5.4.3 Sub threshold Swing/Sub threshold slope(SS

Sub threshold swing or sub threshold slope can be defined as the change in required to change the sub threshold drain current by one decade. It can be expressed as,Sub threshold slope, Sub threshold swing or sub threshold slope can be defined as the change in required to change the sub threshold drain current by one decade. It can be expressed as,Sub threshold slope,

$$SS = \frac{\Delta V_G}{\Delta \log(I_D)}$$

From the above figure, it is observed that the value of SS is low in case of SG NMOS without noise, this is because of less influence of VDS on SG NMOS without presence of noise. So, it identifies that the electrostatic control of gate is more in case SG NMOS without the presence of thermal noise.

5.4.4 Transfer characteristic for DG-MOSFET with and without presence of Thermal noise

The simulated ID-VGS characteristics for both DG with and without noise are shown in Fig.5 (a) and 5(b) at drain bias voltage of VDS=50mV and 0.7V. Making a comparison among Fig. 5(a) and Fig. 5(b), it can be observed that , DG without noise shows a leakage current 10-10 A/m where as DG with presence of noise shows a leakage current which lies in the range 10-9A/m to 10-10A/m.It is also seen that Ioff is low in DG NMOS without noise as compare to DG NMOS with presence of noise.
Hence it can be observed that, DG device without noise has superior performance as compare to DG device with noise because of low leakage current and Ioff .

Table 5.2: Statistical electrical FoMs for DG-NMOS with and without presence of noise VDS=0.05V and 0.7V

DG-NMOS	Threshold Voltage, Vth,VDS=0.05V, VDS=0.7V		DIBL	Ion(A), VDS=VGS=0.7V	Ioff(A), VGS=0V VDS=0.7V	SS(mV/Decade) VDS=0.05V VDS=0.7V	
Without noise	0.245	0.2275	26	0.0010404	1.56408e-10	60.598	60.549
With noise	0.245	0.21	53	0.00105	1.6814e-10	60.597	60.549

DIBL and Ion/Ioff ratio for DG MOS with and without noise

DIBL is low in case of DG-MOSFET without noise (in terms of 26mV/V)as compare to DG with noise(in terms of 53mV/V). This is because of the less influence of VDS on DG without noise configurations. Here Ion/Ioff ratio increases for DG MOS without noise as compare to DG MOS with presence of thermal noise.

Sub threshold Swing/Sub threshold slope(SS)

Sub threshold swing or sub threshold slope can be defined as the change in required to change the sub threshold drain current by one decade. It can be observed that SS is ideal for both the cases.

5.5 Summary

The different electrostatic parameters have been systematically represented for both UTB-SG and DG device with and without effect of thermal noise.From the results, the UTB-SG MOSFET without noise shows an improvement in device performance in terms of SS, DIBL and on-off ratio (Ion/Ioff) over the SG-MOSFET with noise.Similarly, the UTB-DG MOSFET without noise shows an improvement in device performance in terms of SS, DIBL and on-off ratio (Ion/Ioff) over the DG-MOSFET with noise. It can be also observed that DG MOSFET after addition of noise can give better performance as compare to SG MOSFET with effect of noise. So, by analysing and comparing all the parameters, the DG MOSFET is superior in performance shows a higher immunity towards short channel effects.

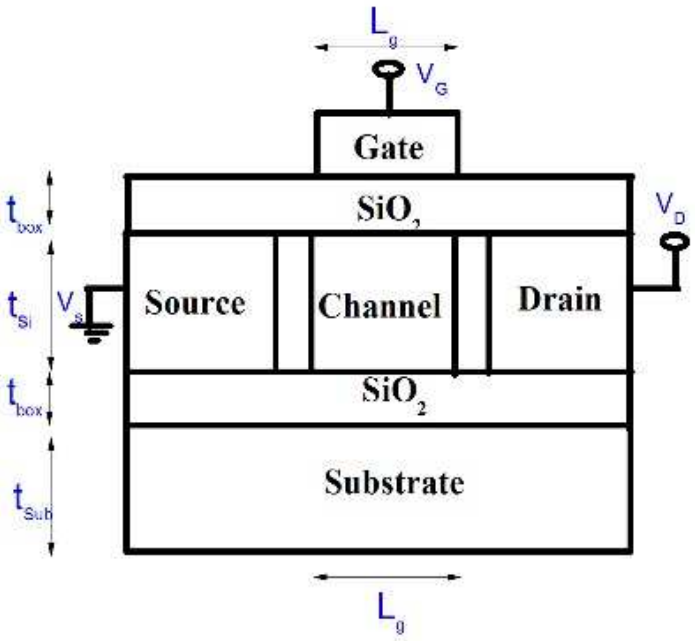

Figure 5.1: UTB-SG MOSFET

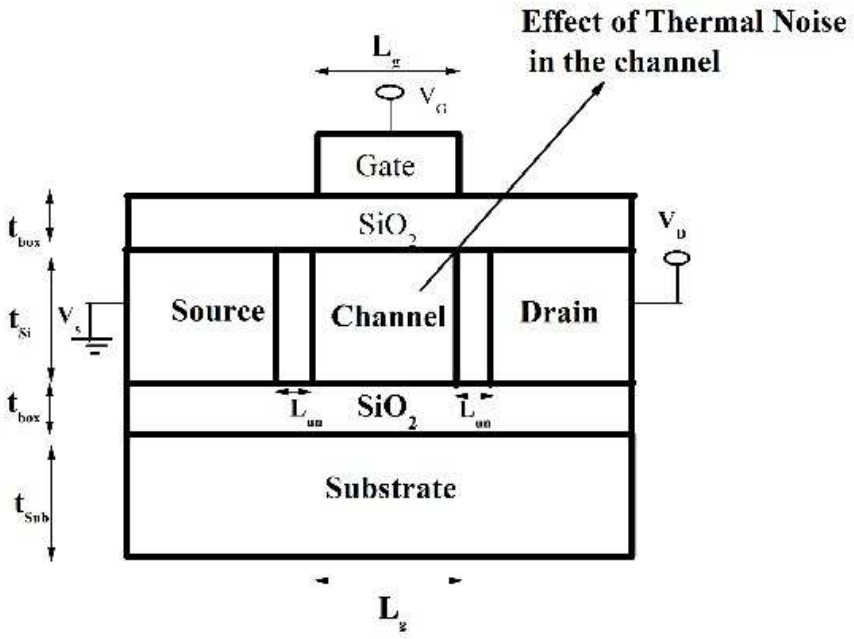

Figure 5.2: UTB-SG MOSFET with presence of Thermal noise.

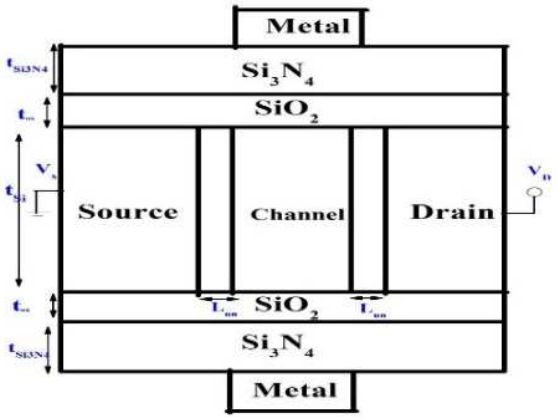

Figure 5.3: UTB-DG MOSFET

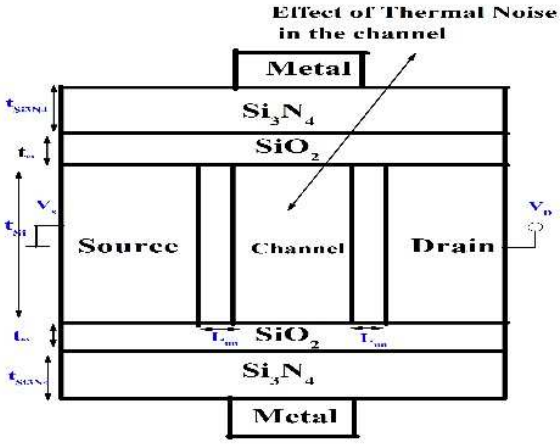

Figure 5.4: UTB-DG MOSFET with presence of Thermal noise

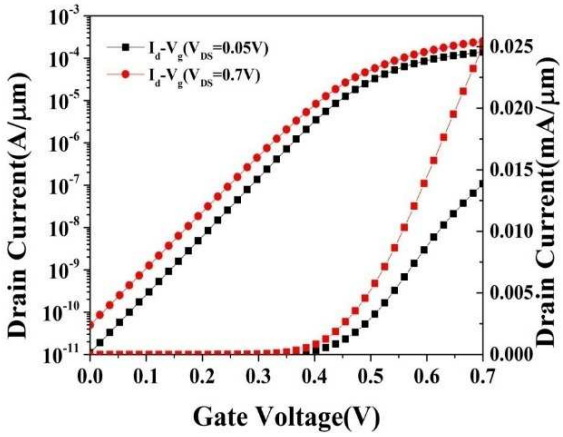

Figure 5.5: SG without presence of noise at VDS=0.05V and VDS =0.7V

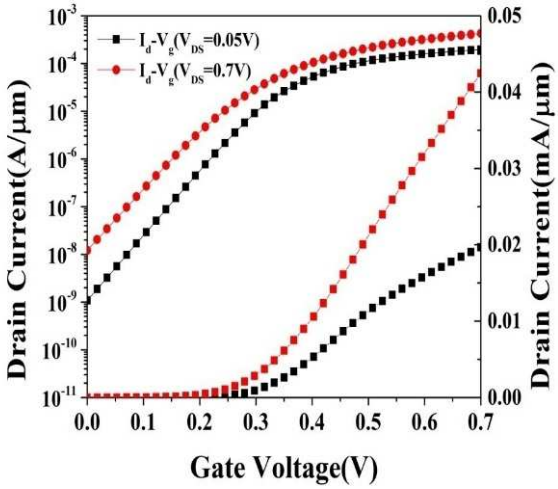

Figure 5.6: SG with presence of noise at VDS=0.05V and VDS =0.7V

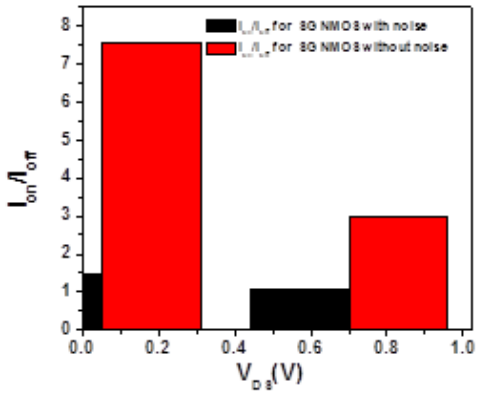

Figure 5.7: The performance metrices for both SG MOSFETs with and without noise at VDS=0.05 V and VDS =0.7V

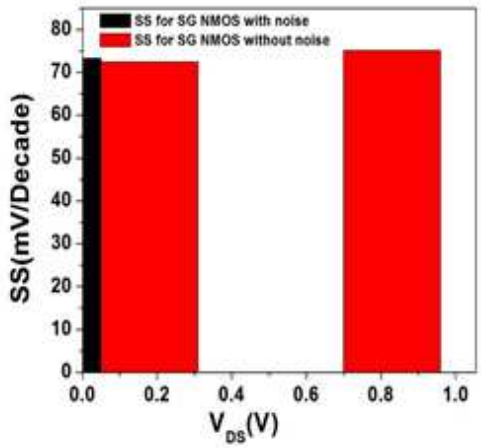

Figure 5.8: SS for SG NMOS with and without noise

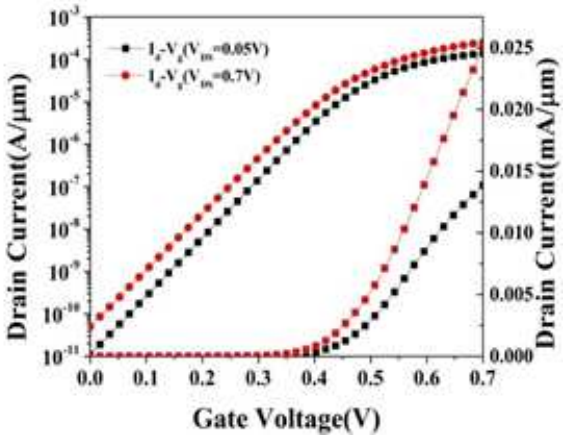

Figure 5.9: DG without presence of noise at VDS=0.05V and VDS=0.07V

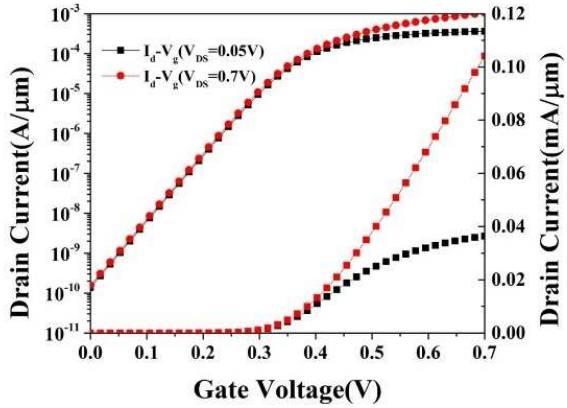

Figure 5.10: DG with presence of noise at VDS=0.05V and VDS=0.07V

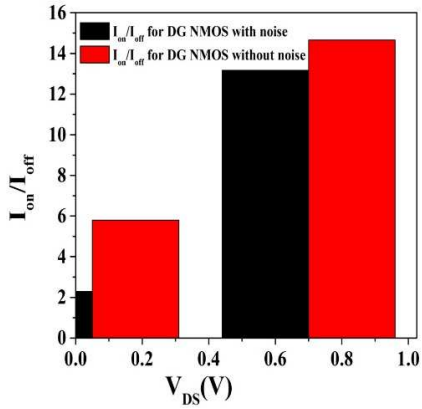

Figure 5.11: The performance metrices for both DG MOSFETs with and without noise at VDS=0.05 V and VDS =0.7V.

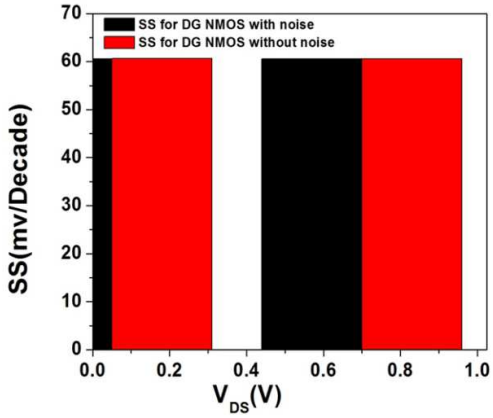

Figure 5.12: SS for DG NMOS with and without noise

Chapter 6

Thermal noise analysis of Single Gate MOSFET at high frequency

6.1 Introduction

Excellent high- frequency behaviour, together with a reduced influence of hot carriers and short channel effects have been claimed for Silicon-on- Insulator (SOI) MOSFETs, thus becoming the mainstream alternative to bulk silicon MOSFETs devices.In particular, the analysis of the noise performance of the transistors is critical in order to develop low-noise applications with a reduced cost. Simulation tools are the best solution to carry out this study, thus helping to further develop silicon technologies[15].
The use of low power, low noise devices for future electronic applications is becoming more and more important. Especially, SOI devices are excellent candidates to become an alternative to conventional bulk CMOS. Advanced MOSFET structures such as ultra-thin-body silicon-on-insulator (SOI) single-gate transistor and the double-gate (DG) transistor can be scaled more aggressively than the bulk Si structures, hence, may be adapted for IC production[23]. A fully depleted double gate (DG) silicon-on-insulator (SOI) is regarded as a near ideal technology, offering a higher drive current than its single gate (SG) counter part due to larger control over channel region, and this strongly enhances the immunity towards the short channel effects (SCEs) and provides an almost ideal sub-threshold slope.However, these advanced structures have distinctly different material is and process technology requirements and associated challenges. Metallic gateelectrodes will be necessary in order for these devices to provide the maximum performance benefit over bulk-Si MOSFETs[**?**].

6.2 Device design

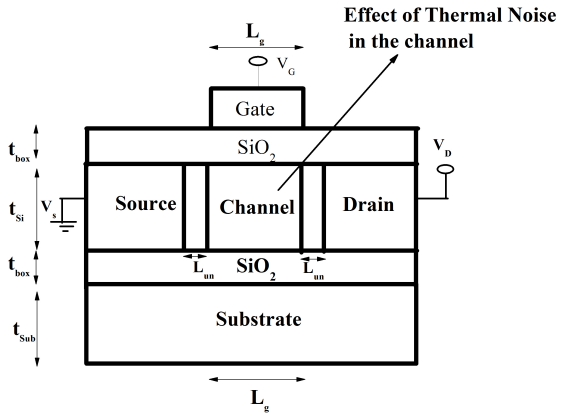

Figure 6.1: Schematic Structure of SG-MOSFET

6.3 Simulation

The simulated devices (Fig.1) consist of UTB-SG MOSFET operating with a power supply voltage of VDD=0.7V. Source/channel and channel/drain junctions are assumed to be abrupt with continuous doping of 1X1015 cm-3 in Source/Drain regions. Different ID-VG characteristics has been done at different drain to source voltage i.e. at VDS=0.05V and 0.7V respectively. The main differences between both structures arise when comparing the induced fluctuations in the gate current: the fluctuations are consistently higher in the double gate structure. The work functions of the metal gates are fixed at 4.5eV to achieve the desired Vth value. The drift-diffusion model is the default carrier transport model in Sentarous device simulator, which is activated in the simulation. In addition the basic mobility model is used to consider the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored in our device simulation[24]. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation.

6.4 Result and Discussion

6.4.1 Variation of Channel length

A typical behaviour of the drain current noise spectral density (Sid) verses drain current (ID), channel length (Lg) and gate to source voltage (VGS) in SGFETs devices is represented in following figure for a measurement frequency (f) of 1MHz.

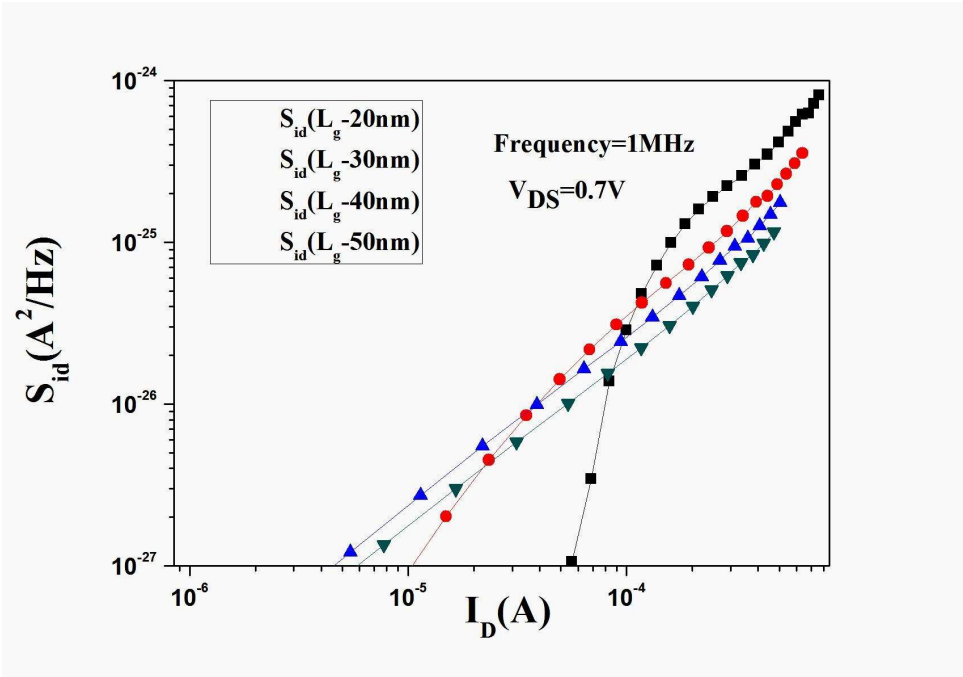

Figure 6.2: Noise Power spectral density variations over I_D

From Figure 6.2 it is observed that Sid follows for low drain currents i.e. quadratic law with the drain current.The dependence of Sid on channel length is represented in Figure 6.3 , where Sid is plotted for n-MOS devices with channel length of L=20, 30, 40,50nm respectively for different VGS, at VDS=0.7V at 1MHz. From Figure 6.3, the value of noise spectral density is more at higher Lg ($L_g = 50nm$) and low for lower value of Lg ($L_g = 30nm$). Here the model predicts a significantly decreased Sid at high gate voltage, particularly for the shorter channel device.
Here the model predicts a significantly decreased Sid at high gate voltage, particularly for the shorter channel device which is shown in Figure 6.4.Without the inclusion of SCEs, the PSD of drain noise current is significantly underestimated. From Figure 6.5 it is observed that the value of Sid/gm2 increases for lower

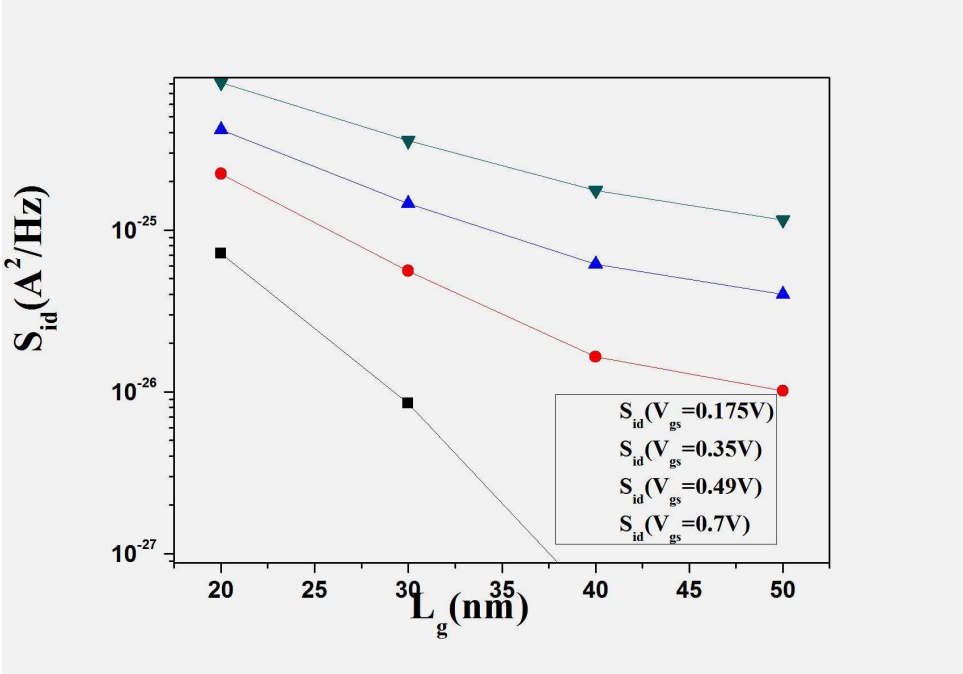

Figure 6.3: Noise Power spectral density variations over L_g with different channel length

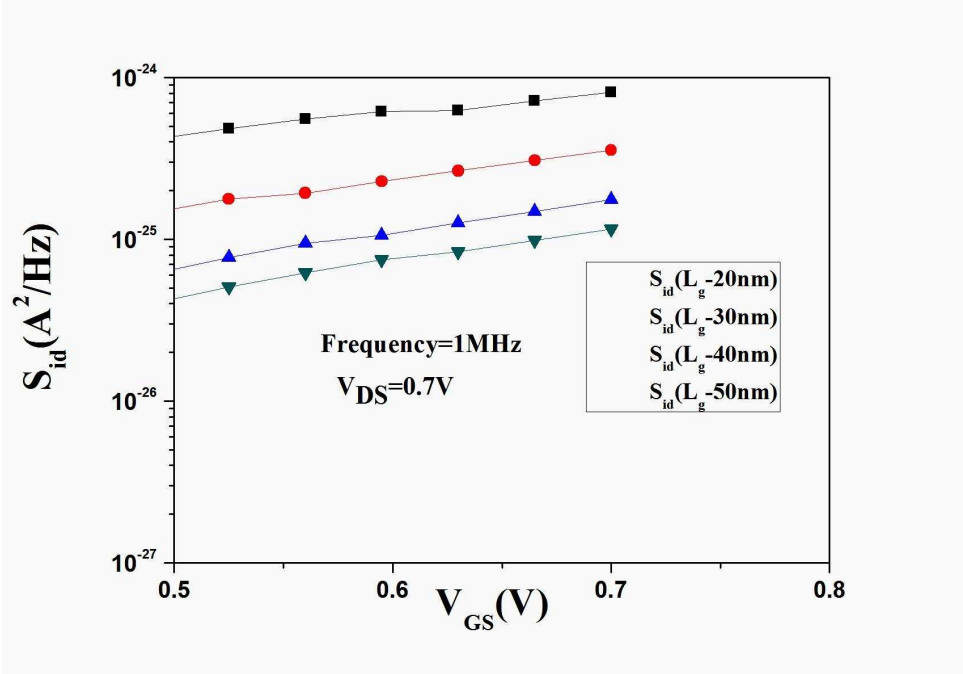

Figure 6.4: Noise spectral density Vs Input-referred voltage noise spectral density(S_{id}/g_m^2) versus gate voltage

Lg (Lg=20nm).With the increase in gate to source voltage, Sid/gm2 decrease. With the increase in drain current, the value of Sid/ID2 decreases which is explained in Figure 6.6. It is also observed from the Fig.3 (c) that the value of Sid/ID2 is high for lower value of Lg (Lg=20nm) and low for higher value of Lg (Lg=50nm).

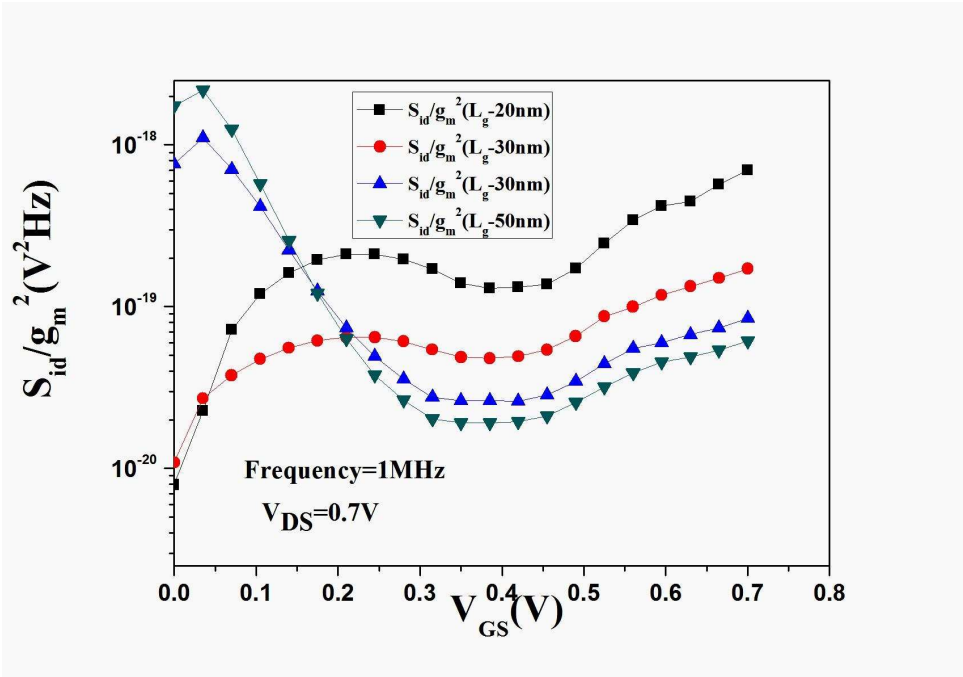

Figure 6.5: Noise spectral density Vs Gate to source voltage Normalized noise spectral density(S_{id}/I_D^2) versus drain current over Lg variation

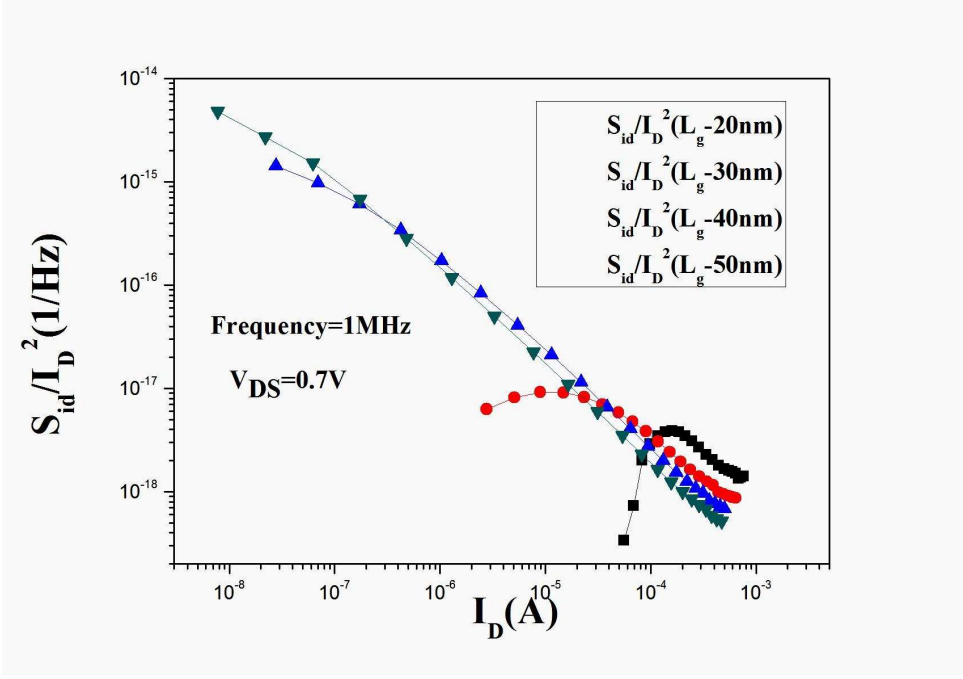

Figure 6.6: Normalized noise spectral density(Sid/ID2) versus drain current over Lg variation

6.4.2 Variation of Silicon thickness

Similar analysis has been done for DG-MOSFET by varying the silicon thickness of the MOSFET.
From the Figure 6.7 it is observed that,noise power spectral density increases with decrease in drain current.With the increase in drain current,the noise signal power increases,so the noise power spectral density increases at constant frequency. The dependence of Sid on silicon thickness is shown in Figure 6.8, where Sid

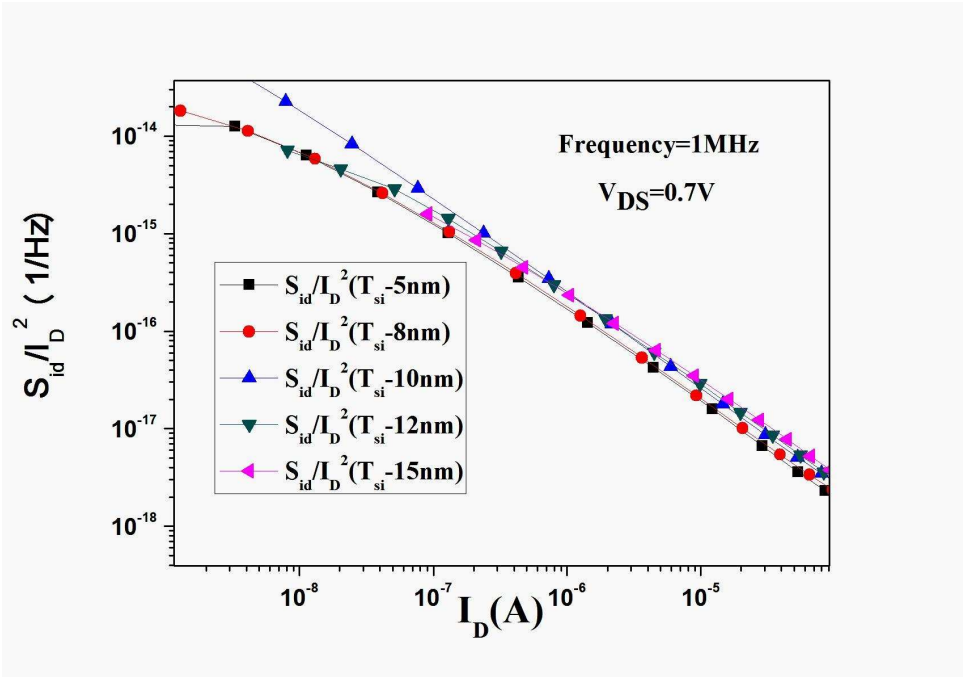

Figure 6.7: Noise Power spectral density variations over I_D

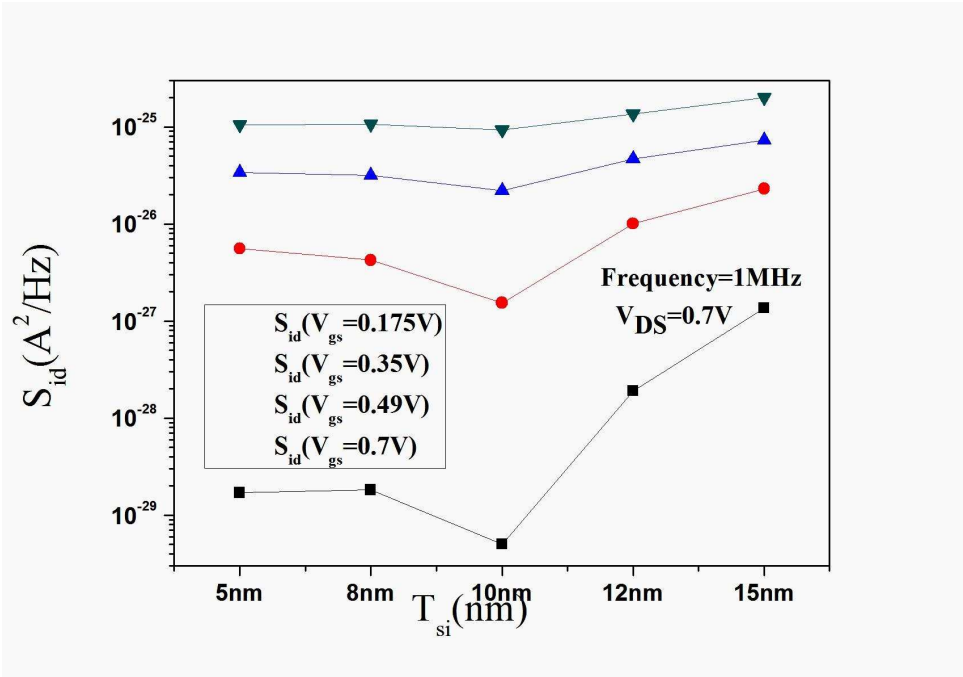

Figure 6.8: Noise Power spectral density variations over $L_g$with different silicon thickness

is plotted for n-MOS devices with silicon thickness of TSi=5,8,10,12,15nm for different VGS at VDS=0.7V at 1MHz. It is shown from Fig.4 (b) that the noise power density is higher for higher TSi and lower for lower TSi.

From Figure 6.9,there is a significant decrease of Sid at high gate voltage. It is also observed thatwhen VS(Velocity Saturation) and CLM(Channel Length Modulation) effects on noise are deactivated (while the dc model remains unaffected,i.e., conserves all SCEs such as VS and CLM),then the model predicts a significantly

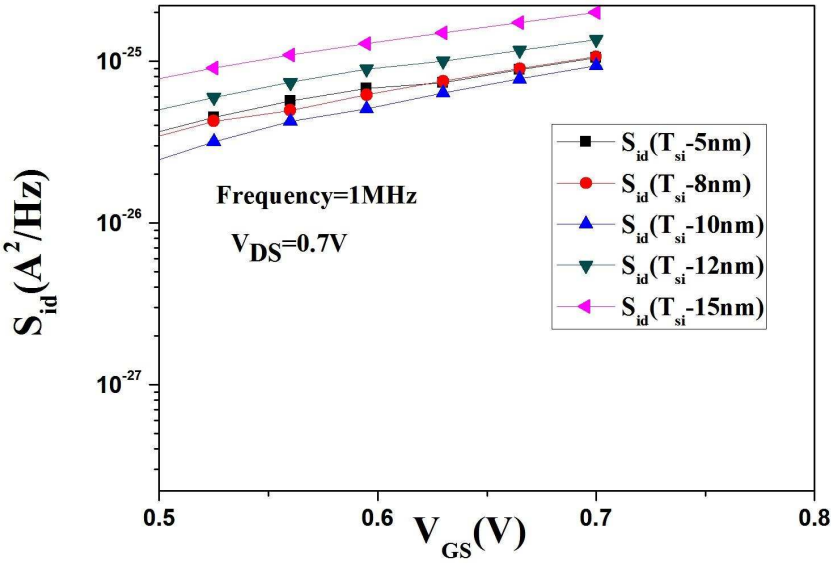

Figure 6.9: Noise spectral density Vs Gate to source Voltage

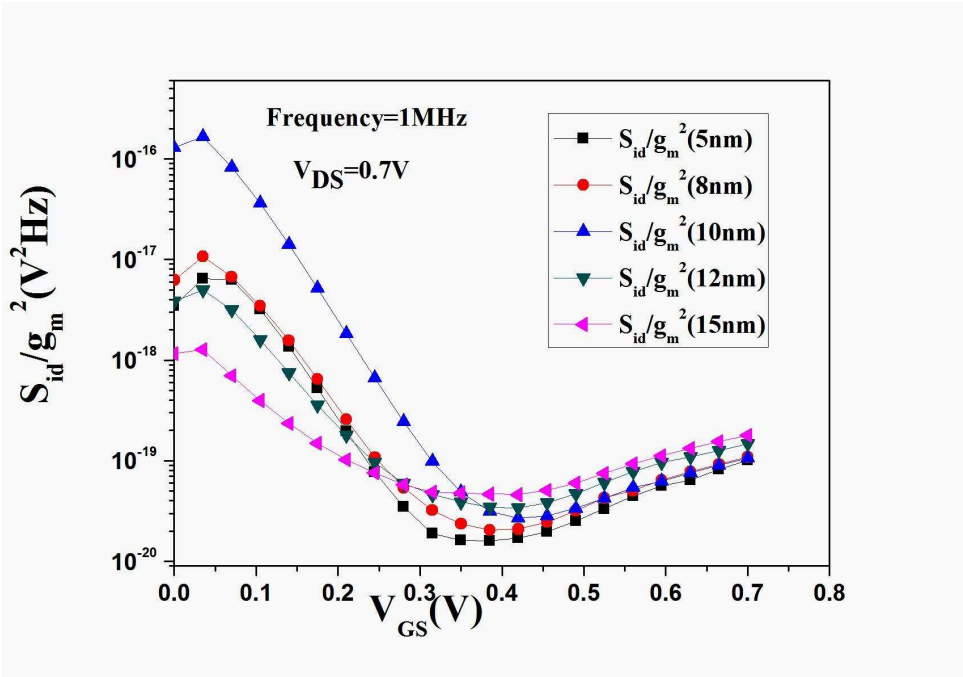

Figure 6.10: Noise spectral density Vs Input-referred voltage noise spectral density(S_{id}/g_m^2) versus gate voltage

decreased Sid at high gate voltage,particularly for the shorter channel device.The value of Sid/gm2 increases for lower TSi which is explained in Figure 6.10. With the increase in Gate voltage,the value of Sid/gm2 decreases. From Figure 6.11, it is shown that with the increase in drain current the value of Sid/ID2 decreases.It is also observed that the value of Sid/ID2 is high for higher value of TSi(TSi=15nm) and low for lower value of TSi(TSi=5nm).

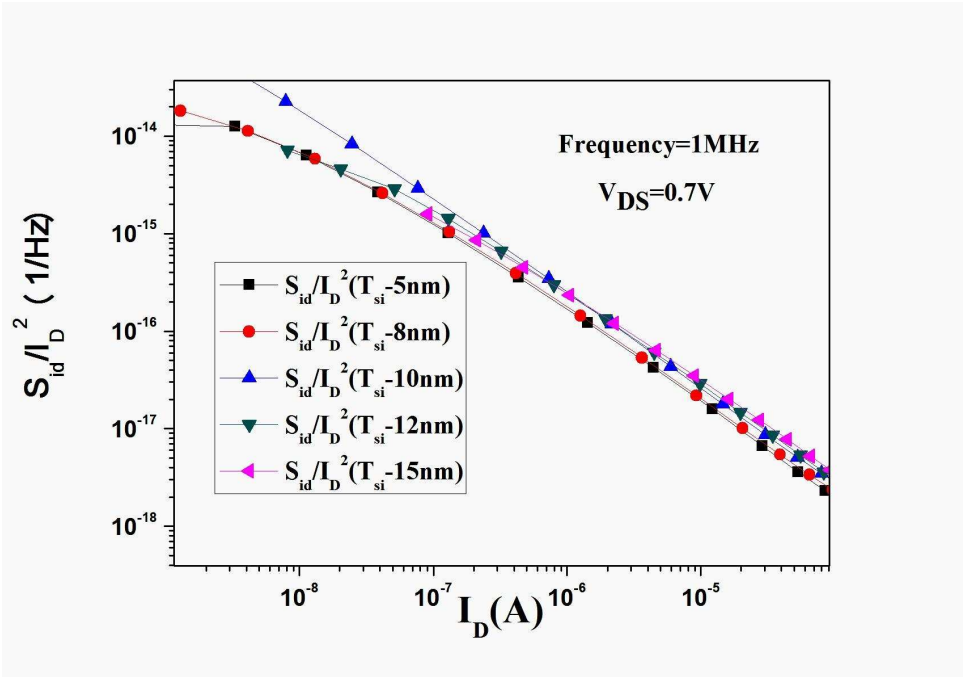

Figure 6.11: Normalized noise spectral density(S_{id}/I_D^2) versus drain current over Tsi variation

6.5 Summary

Here,the analytical drain current model for p-channel SG MOSFET has been discussed and experimentally verified. The charge and drain current are evaluated by considering virtual source, where channel potential is assumed to be minimum. Analysis of thermal noise is made by considering this charge and current results. The variation of the structural parameters such as Lg, and TSi are considered on thermal noise power spectral densities.This work provides an experimental study of the high frequency noise in 2D devices with different channel lengths,and silicon thickness.

Chapter 7

Thermal noise analysis of Double Gate MOSFET at high frequency

7.1 Introduction

Double Gate devices are suitable for nano electronic circuits due to better scalability, higher on-current (Ion), improved Sub-threshold Slope (SS) and undoped body (no random dopant fluctuation). Ultra-thin body (TSi) increases the gate control over the channel resulting in reduced short channel effects (SCEs).Thin Tsi increases the quantum confinement of charge resulting in increased threshold-voltage (Vth), and hence, reduced performance. Further, very thin Tsi poses fabrication challenges and increases device characteristic mismatch due to process variations. In case of UTB FETs, Vth varies with TSi, because of quantum confinement and SCE. Hence, to achieve off state leakage ($V_{GS} = 0V$ and $V_{DS} = 0.7V$) we tune the metal gate work function for each TSi. Reduction of TSi improves the sub threshold slope, hence at off state; Vth reduces resulting in improved on-current. In this work, we have varied the process parameters like channel length and body thickness in presence of thermal noise[25].

7.2 Device design

7.3 Simulation

The simulated devices figure 7.1 consist of DG-MOSFET operating with a power supply voltage of VDD=0.7V. Source/channel and channel/drain junctions are considered to be abrupt with continuous doping of 1x1015 cm-3 in Source/Drain regions. Different noise power spectral density plots have been done at different bias voltages and process parameters. The work functions of the metal gates are fixed at 4.5eV to achieve the desired Vth value [26]. The drift-diffusion model is used as the default carrier transport model in Sentarous device simulator, which is activated in the simulation.The basic mobility model is used to consider the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence[27]. The impact ionization effects are ignored in our device simulation. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation[28].

7.4 Result and Discussion

A typical behaviour of the drain current noise spectral density (Sid) verses drain current (ID), channel length (Lg) and gate to source voltage (VGS) in DGFETs devices is represented in following figure for a measurement frequency (f) of 1MHz. Noise Power spectral denisty can be expressed as,

$$I_{spec} = I_0 * \frac{W_{eff}}{L_{eff}}$$

$$S_{id} = 4KT * \frac{I_{spec}}{U_T} * g_n$$

$$U_T = \frac{KT}{q}$$

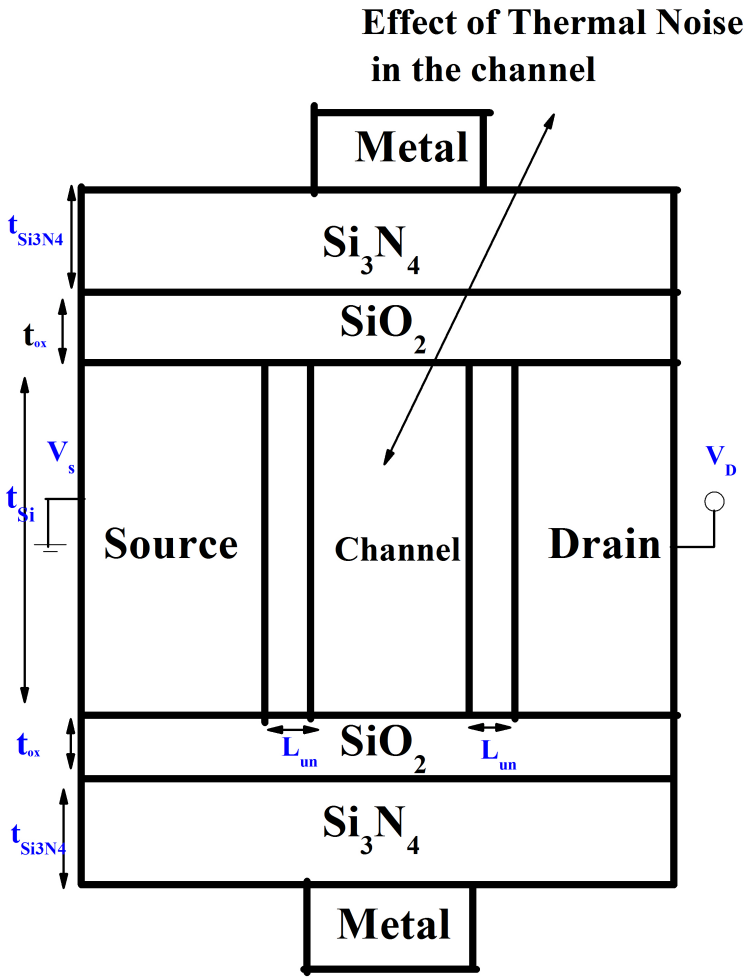

Figure 7.1: Schematic Structure of DG-MOSFET

7.4.1 Variation of Channel length

From Figure 7.2 it is observed that Sid follows for low drain currents i.e. quadratic law with the drain current.The dependence of Sid on channel length is represented in Figure 7.2, where Sid is plotted for n-MOS devices with channel length of L=20, 30, 40,50nm respectively for different VGS, at VDS=0.7V at 1MHz. The slope of the figure is 1/L, as recently explained for longer devices in.It is shown from Figure 7.3, the value of noise spectral density is more at higher Lg (Lg=50nm) and low for lower value of Lg (Lg=30nm). Here the model predicts a significantly decreased Sid at high gate voltage, particularly for the shorter channel device.

Here the model predicts a significantly decreased Sid at high gate voltage, particularly for the shorter channel device which is shown in Figure 7.4.Without the inclusion of SCEs, the PSD of drain noise current is significantly underestimated. From Figure 7.5, it is observed that the value of Sid/gm2 increases for lower Lg (Lg=20nm).With the increase in gate to source voltage, Sid/gm2 decrease. With the increase in drain current, the value of Sid/ID2 decreases which is explained in Figure 7.6. It is also observed from the Figure 7.6 that the value of Sid/ID2 is high for lower value of Lg (Lg=20nm) and low for higher value of Lg (Lg=50nm).

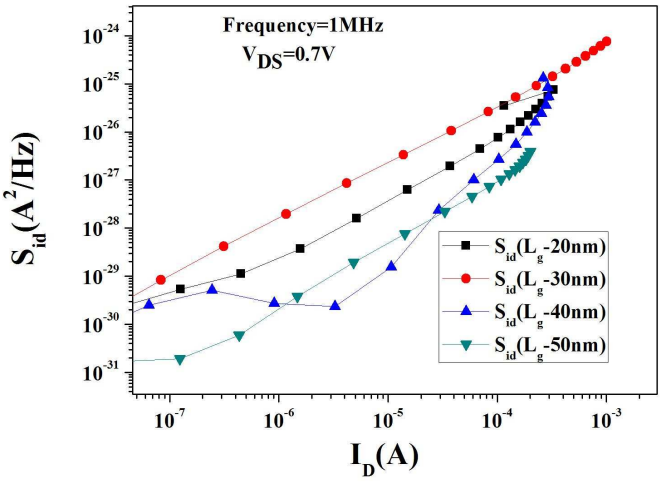

Figure 7.2: Noise Power spectral density variations over I_D

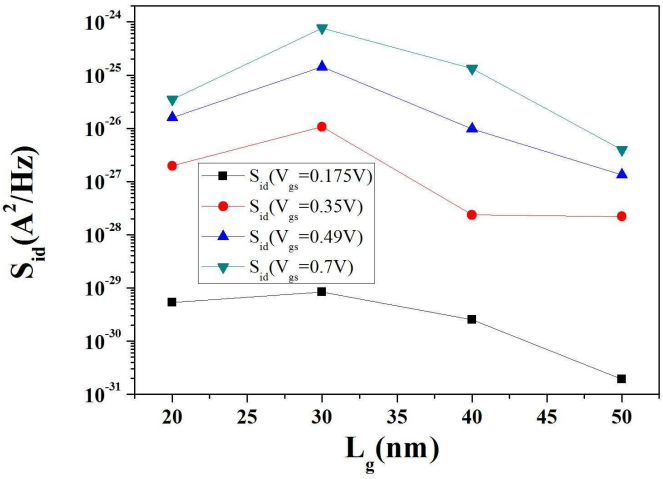

Figure 7.3: Noise Power spectral density variations over different silicon thickness

7.4.2 Variation of Silicon Thickness

Similar analysis has been done for DG-MOSFET by varying the silicon thickness of the MOSFET.
From the Figure 7.7, it is observed that, noise power spectral density increases with decrease in drain current.With the increase in drain current, the noise signal power increases, so the noise power spectral density increases at constant frequency. The dependence of Sid on silicon thickness is shown in Figure 7.8, where Sid is plotted for n-MOS devices with silicon thickness of TSi=5, 8, 10, 12, 15nm for different VGS at VDS=0.7V at 1MHz. It is shown from Fig.4 (b) that the noise power density is higher for higher TSi and lower for lower TSi.
From Figure 7.9,there is a significant decrease of Sid at high gate voltage. It is also observed thatwhen VS(Velocity Saturation) and CLM(Channel Length Modulation) effects on noise are deactivated (while the dc model remains unaffected,i.e., conserves all SCEs such as VS and CLM),then the model predicts a significantly decreased Sid at high gate voltage,particularly for the shorter channel device.The value of Sid/gm2 increases for lower TSi which is explained in Figure 7.10. With the increase in Gate voltage,the value of Sid/gm2 decreases. From Figure 7.11, it is shown that with the increase in drain current the value of Sid/ID2

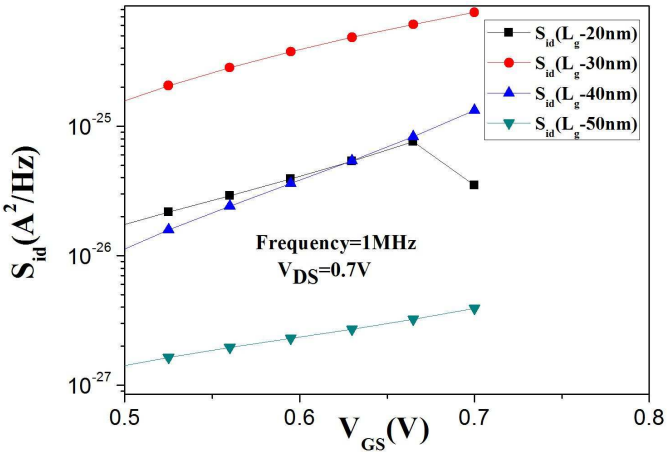

Figure 7.4: Noise spectral density Vs Gate to Source Voltage

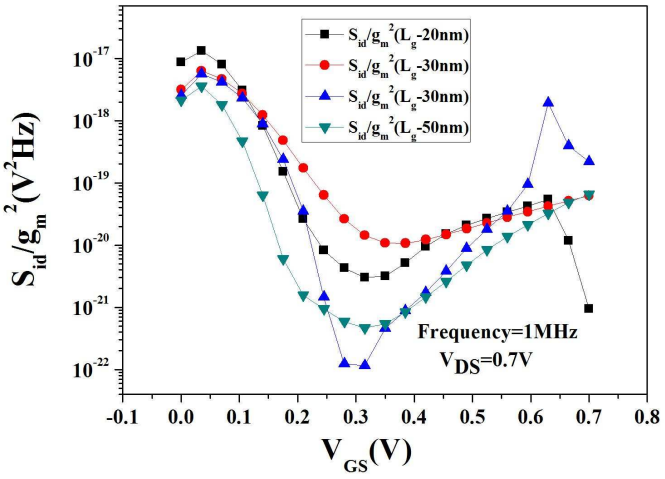

Figure 7.5: Noise spectral density Vs Input-referred voltage noise spectral density(S_{id}/g_m^2) gate voltage

decreases.It is also observed that the value of Sid/ID2 is high for higher value of TSi(TSi=15nm) and low for lower value of TSi(TSi=5nm).

7.5 Summary

Here,the analytical drain current model for p-channel DG Fin FET has been discussed and experimentally verified. The charge and drain current are evaluated by considering virtual source, where channel potential is assumed to be minimum. Analysis of thermal noise is made by considering this charge and current results. The variation of the structural parameters such as Lg, and TSi are considered on thermal noise power spectral densities.This work provides an experimental study of the high frequency noise in 2D devices with different channel lengths,and silicon thickness. The measurements have identified for thermal noise. Thermal noise is produced by random motion of charge carriers due to the thermal excitation. Similarly, it is also observed that with an increase in channel thickness, the volume inversion increases due to electro- static integrity which increases the current, resulting increase in noise power spectral density. However, the noise power

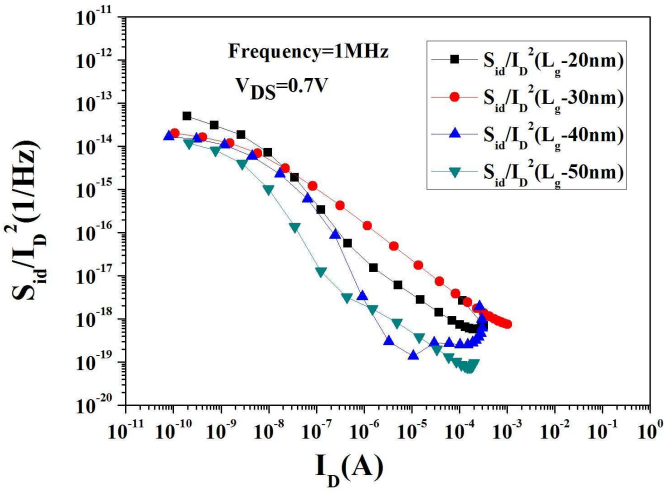

Figure 7.6: Normalized noise spectral density(S_{id}/I_D^2) versus drain current over Tsi variation

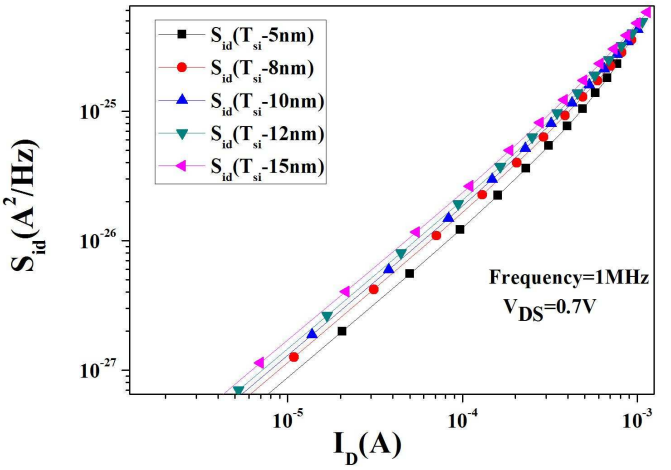

Figure 7.7: Noise Power spectral density variations over I_D

spectral density for the proposed device is very low, which will be very supportive for the low-noise analog RF design at low power supply voltage.

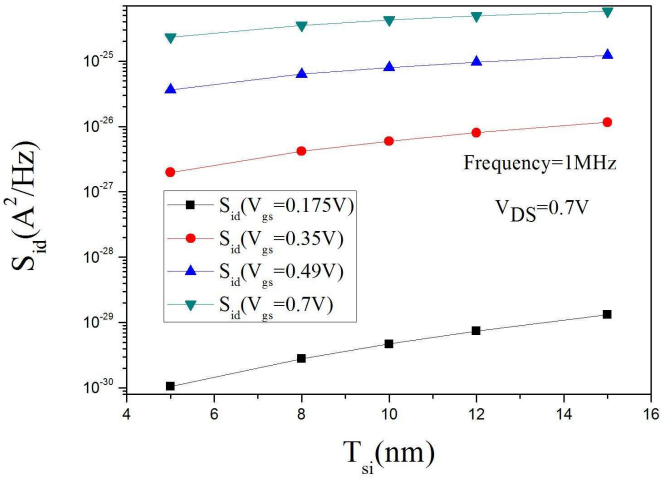

Figure 7.8: Noise Power spectral density variations over different silicon thickness

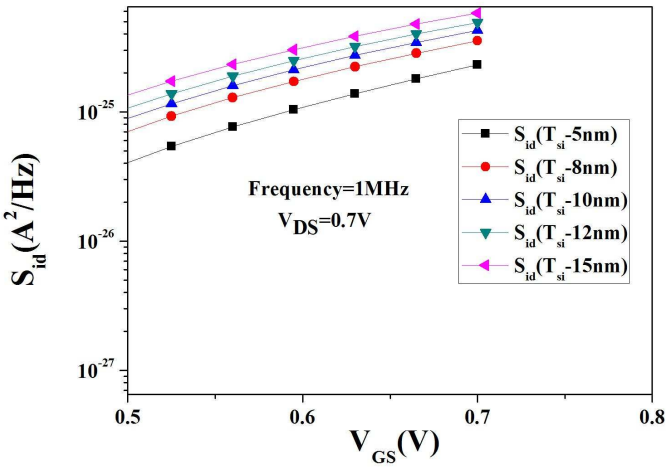

Figure 7.9: Noise spectral density Vs Gate to Source Voltage

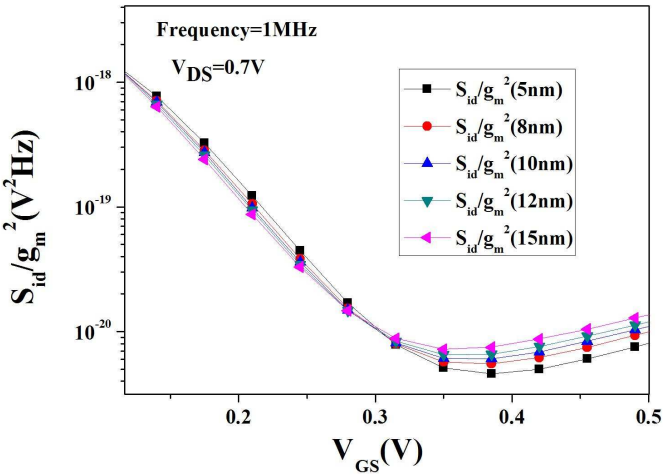

Figure 7.10: Noise spectral density Vs Input-referred voltage noise spectral density(S_{id}/g_m^2) gate voltage

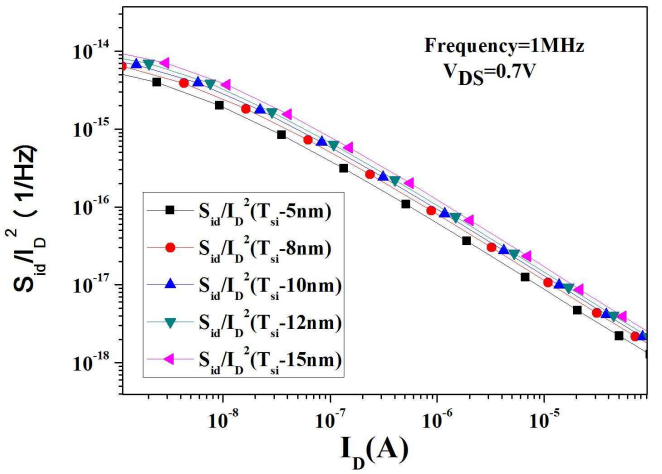

Figure 7.11: Normalized noise spectral density(S_{id}/I_D^2) versus drain current over Tsi variation

Chapter 8

Conclusion and Scope for Future Work

8.1 Conclusion

Continuous scaling in MOSFET devices degrade their performance as a result of leakage currents and short channel effects (SCEs) resulting from downscaling the device dimensions. To mitigate these short channel problems resulting from downscaling the device dimensions a device called Silicon-on-Insulator (SOI) MOSFET has been developed. From the results, the UT-SDOI DG shows a higher drive current and lower DIBL than its counterpart UT-SDOI SG even maintaining a constant Ioff. The on-off current ratio for SDOI DG increases around a factor of 4 than SDOI SG in case of NMOS and a factor of 3 in case of PMOS case. From all analysis UT-SDOI DG MOSFET has potential to meet the ITRS roadmap for 22nm technology node and below this node with considerable amount of design flexibility for HP and LOP devices are achievable. With the use of high mobility channel materials (GaAs, In0.53Ga0.47As) in DG MOSFET, we have found that a strong decrease of DIBL in GaAs and In0.53Ga0.47As. Our result shows that In0.53Ga0.47As based DG MOSFETs have the lower DIBL, but is the most impacted by quantum confinement effects. So by comparing these parameters, DG MOSFET with high mobility materials exhibits high drive current which is more suitable for better switching application. In presence of thermal noise, SG MOSFET performance decreases.It is also observed in DG MOSFET that in presence of thermal noise, with an increase in channel thickness, the volume inversion increases due to electro- static integrity which increases the current, resulting increase in noise power spectral density. However, the noise power spectral density for the proposed device is very low, which will be very supportive for the low-noise analog RF design at low power supply voltage.

8.2 Scope for Future Work

The research work carried out in this thesis has proved the ability of reducing short channel effects and improving the device performance in terms of Analog/RF applications by choosing appropriate device dimensions with suitable materials. This thesis has presented the AC and noise behaviours of deep-sub-micron MOS transistors, however, as the size of the MOS devices continue scale down aggressively, there are still many challenging topics for research. Several recommendations for future research will be discussed here. The channel length of a MOS transistor will eventually be reduced to tens of nanometre range. This size of short channel length will be comparable to the carrier mean free path, which is in the several nanometre range. Therefore, the local noise at each point will have a correlation with that of another location. This effect creates another uncertainty of noise performance in MOS transistors. Currently, no significant investigation or measurement has been performed on this matter.

List of Publication

- D. Singh, S. Panda, S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, Static performance analysis on UTB-SG and DG MOSFETs with Si and III-V channel materials, IEEE international conference ICHPCA, Bhubaneswar, 2014.
- S. K. Mohapatra, K. P. Pradhan, P. K Sahu, D Singh, S. Panda, Ultra-Thin Si Directly on Insulator (SDOI) MOSFETs at 20 nm gate length, IEEE international conference ICHPCA, Bhubaneswar, 2014.

- S. Panda, D. Singh, P. K. Sahu, S. K. Mohapatra, K. P. Pradhan, Impact of LAC doping and metal gate work function on Performance of GS-DG-MOSFETs, IEEE conference AEDAC ,Bhubaneswar,2014.
- D. Singh, S. Panda, S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, performance comparison between Ultrathin body(UTB) single and Double gate MOSFETs,International conference on Micro- electronics, Communication and Computation, ICMCC,SAN DIEGO,USA 2015. (Got best paper Award)

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